East Eur. J. Phys. **3**. 71-80 (2019)
DOI:10.26565/2312-4334-2019-3-09

PACS: 61.05.cp, 61.43.Dq, 61.72.Yx, 61.72.Mm, 61.82.Fk, 68.37.Hk, 68.55._a, 85.30.Tv

ELECTRIC DOUBLE LAYER FIELD EFFECT TRANSISTOR USING SnS THIN FILM AS SEMICONDUCTOR CHANNEL LAYER AND HONEY GATE DIELETRIC

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Received July 24, 2019; revised September 3, 2019; accepted September 26, 2019

The study aimed at the investigation and application of SnS thin film semiconductor as a channel layer semiconductor in the assembly of an electric double layer field effect transistor which is important for the achievement and development of novel device concepts, applications and tuning of physical properties of materials since the reported EDLFET and the modulation of electronic states have so far been realised on oxides, nitrides, carbon nanotubes and organic semiconductor but has been rarely reported for the chalcogenides. Honey was used as a gel like electrolytic gate dielectric to generate an enhanced electric field response over SnS semiconductor channel layer and due to its ability to produces high on-current and low voltage operation while forming an ionic gel-like solution similar to ionic gels which consist of ionic liguids. SnS gated honey Electric double layer field effect transistor was assembled using tin sulphide (SnS) thin film as semiconductor channel layer and honey as gate dielectric. The measured gate capacitance of honey using LCR meter was measured as 2.15 μF/ cm^2 while the dielectric constant is 20.50. The semiconductor layer was deposited using Aerosol assisted chemical vapour deposition and annealed in open air at 250℃ on an etched region about the middle of a 4×4 mm FTO glass substrate with the source and drain electrode region defined by the etching and masking at the two ends of the substrate. Iridium was used as the gate electrode while a copper wire was masked to the source and drain region to create electrode contact. The Profilometry, X-ray diffraction, Scanning electron microscope, Energy dispersive X-ray spectroscopy, Hall Effect measurement and digital multimeters were used to characterise the device. The SnS thin film was found to be polycrystalline consisting of Sn and S elements with define grains, an optical band of 1.42 eV and of 0.4 μm thickness. The transistor operated with a p type channel conductivity in a depletion mode with a field effect mobility of 16.67 cm^2/Vs, cut-off voltage of 1.6 V, Drain saturation current of1.35μA, a transconductance of -809.61 nA/V and a sub threshold slope of -1.6 $Vdec^{-1}$ which is comparable to standard specifications in Electronics Data sheets. Positive gate bias results in a shift in the cut off voltage due to charge trapping in the channel/dielectric interface.
KEY WORDS: SnS thin film; Field effect transistor; Honey; Electric double layer; semiconductor

A transistor is a three terminal semiconductor solid state device used for the amplification and switching of electronic signals. Transistors are classified into bipolar junction transistors (BJT) and the field effect transistors (FET) [1]. The field effect transistor utilises only the majority charge carriers for electrical conduction. The FET consist of a source electrode, drain electrode, gate electrodes and a semiconductor active channel region such that an applied electric field via the gate voltage is used in controlling the channel conductivity with a flow of charge carriers from the source electrode to the drain electrode [2].

An electric double layer may be defined as a nano gap capacitor with a large specific capacitance which on application of low gate voltage can electrostatically modulate the semiconductor channel layer of a field effect transistor by the accumulation of electric charge carriers at the interface between the semiconductor layer and the gate dielectric [3]. An electric double layer field effect transistor (EDLFET) with an advantage of reduce operational voltage due to such a large specific capacitance could be formed from the nano gap electric double layer capacitor by the replaced of one of the capacitor's electrode with a semiconductor material alongside the other electrodes in the capacitors configuration [4].

Electric double layer field effect transistors are of emerging interest in the mimicking of biological synaptic functions, electric control of ferromagnetism, signal processing and sensing in medical physics which requires a low operational voltage and high charge carrier concentrations [5]. The operation of a field effect transistor with a low operating voltage and higher carrier concentration is essentially dependent on the choice of semiconductor channel layer material and the gate dielectric among other parameters since the threshold voltage (V_{th}), which is the voltage required in switching a transistor is dependent on the semiconductor material [3] and also the minimum gate to source voltage differential that is needed to create a charge carrier conducting path between the source and drain is dependent on the semiconductor channel layer in an EDLFET.

However, the reported EDLFET and the modulation of electronic states have been so far realised only on oxides, nitrides, carbon nanotubes and organic semiconductor. Therefore, the application of the electric double layer field effect transistor technique to other semiconductor materials has become one of the emerging interests for novel electronic phenomena. This trend is increasingly important for the achievement and development of novel device concepts, applications and tuning of physical properties of materials [5].

Metal chalcogenides (MX-where M denote metal (usually transition metal) and X denote chalcogen) such as Tin(II) sulphide (SnS) and metal dichalcogenides (MX_2, where M and X denote metal and chalcogen respectively) such as

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Tin(IV) sulphide (SnS_2) are of interest as potential candidates for the transport channel of EDLFET. Chalcogenides are materials containing a transition element and one or more chalcogen elements (Silicon, Selenium, Polonium and Tellunum). They found vital applications in solar cells, photoconductive
materials, thermoelectric materials, rewritable memory, studying of dopant induced superconductivity, charge density formation and transistors. SnS is abundance in the earth's crust, SnS is one of the Tin chalcogenides semiconductors, it possess the an orthorhombic crystal structure, it has good air stability, the constituent elements are abundant in nature and not expensive [6], it is not toxic; it is a mostly a p type semiconducting material with carrier concentration on the order of $10^{16}cm^{-3}$, hole mobility of 1.4 $cm^2V^{-1}s^{-1}$ and low resistivity [7]. The SnS is relatively unexplored for application in electric double layer thin film field effect transistor, as existing literatures on the application of SnS thin film as semiconductor channel of an electric double layer field effect transistor is relatively scanty or not available. Hence the SnS thin film is a potential semiconductor to test the feasibility of the chalcogenides as a semiconductor channel layer for application in an electric double layer field effect transistor.

Consequently, the article focuses on the use of SnS as a channel layer in an EDLFET and honey as the gate dielectric. Honey was reported to possess the ability to produces high on-current and low voltage operation while forming an ionic gel-like solution similar to ionic gels which consist of ionic liguids. It has recently shown ideal transistor performance as a electrolytic gate dielectrics in Graphene field effect transistors using liquid metal interconnects [8].

MATERIALS AND METHOD

For the assembling of SnS EDLFET, FTO glass substrate was cleaned using the cleaning methods described as follows: **a.** the substrates were washed in sodium lauryl sulphate (SLS) solution to remove oil and protein. **b.** To remove the organic contaminants, the substrates were immersed in piranha solution (H_2SO_4: H_2O_2 (3:1)) for 30 minutes. **c.** The substrates were then ultrasonically cleaned in distilled water using a sonicator and kept in methanol until it is ready to be used. **d.** Finally, to use the substrate for deposition process, the substrate were taken from the methanol and dried in air at 150°C after which it was used for the assembling of the SnS EDLFET. A 4×4 mm FTO glass was masked (from both ends to create the drain and source contact respectively) and then etch about the middle using Zinc powder and Hydrochloric acid as the etchant in order to create the semiconductor channel region. A 0.40 µm SnS thin film was deposited on the etch region with a channel length of 70 µm and channel width of 4000 µm by AACVD to serve as the semiconductor channel layer. The SnS semiconductor channel layer was deposited using 0.1 M Tin chloride dehydrates (BDH) and 0.2 M of Thiourea (BDH) which was weighed in stoichiometric proportion and dissolve in ethanol solvent. The two solutions were mixed and stirred for 1 hour using a magnetic stirrer at room temperature, after which the resulting solution was filtered through a 0.22 µm syringe filter and then deposited on the substrate by aerosol assisted chemical vapour deposition (AACVD) at a constant substrate temperature of 258 °C, nozzle distance of 6.8 mm, substrate to nozzle distance of 3 cm, spray volume of 0.2 mL and spray rate of 0.04 ml/min. With the Drain and Source region still masked, the deposited SnS thin film semiconductor channel layer was annealed in open air at annealing temperature of 250°C for one hour after which it was allowed to cool to room temperature before undergoing characterisation.

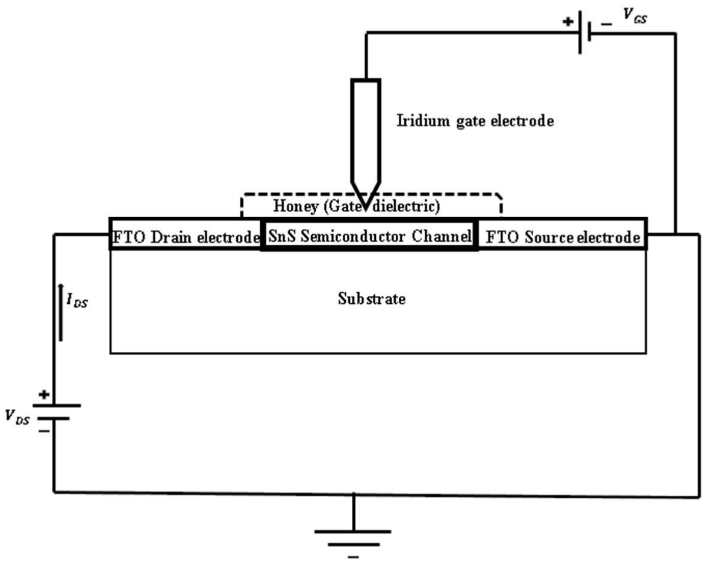


Fig. 1. A schematic diagram of the SnS EDLFET

The FTO drain and source contacts were bonded with a thin copper wire after which Honey which was commercially acquired was dispensed from a plastic dropper at a volume of 150.59 mm^3 and 136.90 mm^2 surface area of the SnS thin film semiconductor channel layer between the source and drain to act as the electrolytic gate dielectric after which an Iridium (Ir) electrode was suspended above the SnS channel layer, but inside the honey gate dielectric to act as the gate electrode. These were all placed in a transparent Glass container. The electric measurements was then carried out at room temperature using two variable power supplies (KOOCU DC Power supply 1502DD with voltage variation of 0-15 V and ATX-650W, hp invent with voltage variation of 0-12 V) and two digital multimeters (CHY VC 890C$^+$ digital Multimeter and DT9205ACE digital Multimeter). The V_G applied to the Ir electrode was scanned from 0 to 1 V by 0.2 V step. The quality of the EDLFET was determined by measuring the gate current Ig for a gate voltage Vg. A schematic of the SnS EDLFET is shown in Fig. 1.

CHARACTERISATION TECHNIQUES FOR THE DEPOSITED SNS THIN FILM

The crystal phase analysis was carried out at room temperature using an X-ray diffractrometer (D8 Advance, Bruker AXS, 40Kv, 40 mA) with monochromatic CuKα (λ=1.540598 Å) over a scan mode of step size 0.034° and counts accumulated for 192.1 s at each step for 2θ ranging from 20° to 80°. The XRD diffractogram was obtained using Origin Pro 2018 software with the FWHM for the peaks estimated using a Gaussian function. Results was analysed with the scientific graphing analysis software and phase identification was done using the inorganic crystal structure data (ICSD) pattern [9].

The lattice parameters a, b and c value for the orthorhombic crystallographic system of Tin (II) sulphide thin film was calculated from the observed values of 2θ using d values (interplaner spacing) for the orthorhombic structure [10]:

$$1/{d^2}_{hkl} = h^2/a^2 + k^2/b^2 + l^2/c^2. \quad (1)$$

XRD pattern of the film was first indexed after which three peaks whose (hkl) is known were selected and resolved for a, b and c lattice constants of the SnS thin film which is also equivalent to:
$a = \frac{1}{d_{101}} = \frac{bcsin\alpha}{V}$; $b = \frac{1}{d_{040}} = \frac{acsin\beta}{V}$; $c = \frac{1}{d_{002}} = \frac{absin\gamma}{V}$. Where V (unit cell volume)=abc (for orthorhombic), d is the space between lattice planes, h k l are the miller indices while α, β, γ are the diffraction angles.

The inter atomic spacing d was calculated from the Bragg's equation [11]:

$$2d\sin\theta = n\lambda, \quad (2)$$

$$d = \frac{\lambda}{2sin\theta}. \quad (3)$$

Where n=1, λ=1.5406A^0

The average crystallite size of the film was calculated using Debye Scherer's formula [11] assuming spherical crystallite: Crystallite size $=\frac{K\lambda}{\beta Cos\theta}$, which can also be written as

$$D = \frac{0.9\lambda}{\beta cos\theta}. \quad (4)$$

Where β = full width at half maximum (FWHM), θ = diffraction angle, k = Shape factor and λ = wavelength of the X-rays (1.5406 Å) and D= grain size respectively.

Dislocation density δ was calculated using the equation [12]:

$$\delta = \frac{1}{D^2}. \quad (5)$$

Where D is the grain size of the film. The micro-strain ε was estimated using the equation [13]:

$$\varepsilon = \frac{\beta}{4tan\theta}. \quad (6)$$

Quantitative information about the preferential crystallite orientation of the SnS thin films was obtained from the texture coefficient (TC) which represents the preferential growth of certain planes compared to randomly oriented crystallites and was determined from the relation [14-15]:

$$TC = \frac{I/I_o}{(1/N)\Sigma_N(I/I_o)}. \quad (7)$$

Where: I is the measured intensity of the intense peak in the XRD spectrum, I_o is the intensity for completely random sample or the standard intensity of the hkl plane taken from the JCPDS 00-039-0354 card and N is the number of reflections considered in the analysis.

The morphology and the microstructure of the SnS thin film was characterized using High Resolution Scanning Electron Microscopy (HR-SEM, Zeiss) while the elemental composition of the films were determined by an Energy dispersive X-ray spectroscopy (EDS; Oxford instrument) attached to the SEM . The instrument was operated at a voltage of 20 kV while the images were captured at 5 kV. A Profilometry (VEECO DEKTAK 150) was used to carry out measurement of the thickness of the deposited films.

Electrical Characterisation

The carrier density, carrier mobility and carrier type were determined by an ECOPIA Hall Effect measurement system (HMS 3000 Hall measurement system) based on Van der pauw configuration. Two variable power supplies (KOOCU DC Power supply 1502DD with voltage variation of 0-15 V and ATX-650W, hp invent with voltage variation of 0-12 V) and two Multimeter (CHY VC 890C$^+$ digital Multimeter and DT9205ACE digital Multimeter) were also used to determine the electrical behaviour of the fabricated transistor. The temperature dependent resistance measurement of the deposited film was carried out in the temperature range of 283 to 523 K.

Evaluation of device performance of the fabricated EDL field effect thin film Transistor

The electrical behaviour of the SnS channel EDL field-effect transistors was evaluated by the plot of drain current (I_D) versus the drain-source bias which is called the output characteristics and the gate-source bias (V_{GS}) which is called transfer characteristics. To evaluate the device performances, electrical parameters such as field-effect mobility (μ_{FE}), cut off voltage, drain saturation current threshold voltage (V_{th}), transconductance and sub threshold swing (SS) were mainly considered as follows:

The x-axis value at the intercept of the transfer curve gives the value of Gate to source cut-off voltage ($V_{GS\,(OFF)}$) while the y-axis intercept gives the drain saturation current(I_{DSS}). The transconductance (g_m) which is simply the slope of the transfer characteristics was calculated using [1]:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}. \tag{8}$$

The field effect mobility μ_{FE} was also obtained from the transconductance at low V_{DS} by:

$$\mu_{FE} = \frac{L g_m}{W C_i V_{DS}}. \tag{9}$$

Where C_i is the capacitance per unit area of the gate dielectric, w is the device width while L is the device length. The mobility is the average drift speed of carriers under the unit electric field.

The sub threshold swing (SS) which reflects the necessary V_G required to increase I_{DS} by an order of magnitude in the sub threshold region ($V_{GS} < V_{th}$) was determined as the inverse of maximum slope of the transfer curve given as:

$$SS = \left(\frac{d\log(I_{DS})}{dV_{GS}}\right)^{-1} \tag{10}$$

RESULTS AND DISCUSSION

Compositional analysis of the annealed SnS thin film

The thickness of the SnS thin film was measured to be 0.40 µm thickness from the profilometry result. The main constituents' elements and their relative concentrations are given in table 1.The annealed SnS thin film was brown in colour, smooth, pin hole free and adheres firmly to the glass substrate surface. No significant colour change was noticed with annealing of the firm.

Table 1

SnS thin film elemental composition (atomic percent) at varied annealing Temperatures.

Annealing Temperature (°C)	Sn (at.%)	S (at.%)	Sn/S at %ratio	SnS (Total)
250	37.28	62.72	0.594	100

Fig. 2 gives the EDX spectrum of the SnS thin film deposited at annealing temperature of 250°C. From the figure, it is evident that the film contained Tin (Sn) and Sulpur (S) elements. However Na, Ca, Si, Cl and Ca elements were also observed which could be attributed to the glass substrates used. Similar observation was also made by [10,16]. The relative concentrations of Sn and S on the samples were evaluated as given in table 3.1 and by the EDS spectrum.

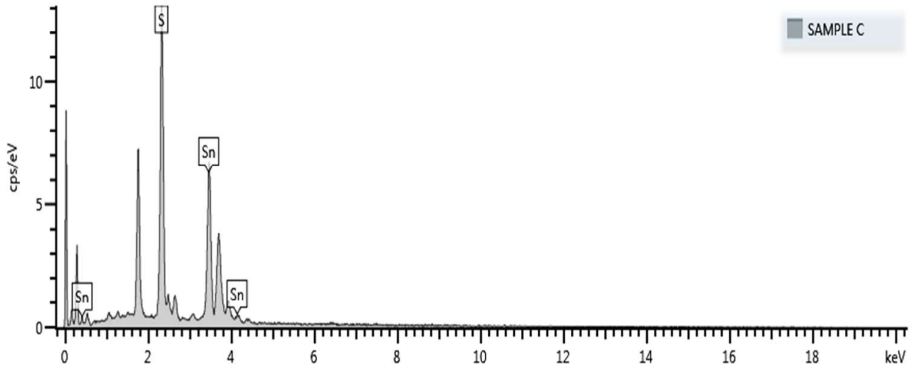


Fig. 2. EDS spectrum of the SnS thin film semiconductor channel layer

XRD Analysis

Fig. 3. shows the XRD pattern of SnS thin film annealed at 250 °C annealing temperature. The XRD spectra of SnS thin film annealed at annealing temperature of 250 °C is shown in fig 3 where the peaks which were identified using the JCPDS card number 39-0354 data are labelled with corresponding orientations using the miller indices. All reflections were indexed to orthorhombic SnS phase as compared with the standard JCPDS card. The X-ray diffractogram or

spectrum of the annealed film exhibited peaks of different orientations at 2Θ values of approximately 29.3°, 31.7°, 45.5° and 62.1° corresponding to (101), (040), (002) and (202) peaks. No impurities peaks of elemental sulphur, tin or other tin sulphide phases were identified in the XRD pattern of the annealed films which buttress the formation of pure SnS phase. The annealed SnS films were polycrystalline and showered an orthorhombic structure with calculated lattice parameters of a= 0.429 nm, b=1.123 nm and c=0.399 nm and an observed d spacing of 2.8194 (°A). The calculated texture coefficient values of the SnS semiconductor channel layer is given in Table 2.

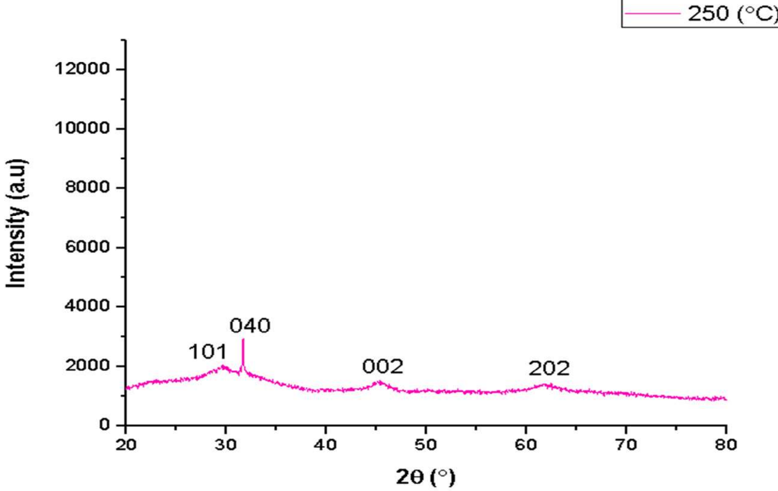


Fig. 3: XRD pattern of the SnS thin film semiconductor channel layer

Table 2.
Texture coefficient value for the SnS semiconductor channel laye

S/N	Annealing Temperature °C	Texture coefficient (TC)				
		TC(101)	TC (040)	TC(002)	TC (202)	TC(080)
1	250	0.46	2.52	0.50	0.51	0

The value obtained shows that the TC value of (040) plane of annealed SnS semiconductor channel layer component are larger than 1 which reveals that the SnS thin film is polycrystalline with preferred orientation along the (040) plane denoting that the number of crystallite and grains along this plane is more than that on the other planes [14, 15, 17]. The peak associated with the (040) plane was used to calculate the crystallite size and other structural parameters been the preferred orientation of the annealed SnS thin film. The calculated average crystalline size, dislocation density and micro strain for the film is shown in Table 3.

Table 3.
Average crystalline size, dislocation density and micro strain for the SnS semiconductor channel layer

S/n	Annealing Temperature (°C)	Full width half maximum $\boldsymbol{\beta}$ (°)	2Θ (°)	Grain size D (nm)	Dislocation density $\boldsymbol{\delta} \times \mathbf{10^{14}}$ (Lines/$\boldsymbol{m^2}$)	Micro strain $\boldsymbol{\varepsilon} \times \mathbf{10^{-4}}$
1	250	0.12644	31.71153	65.30	2.35	5.31

The large average crystallite size obtained could also be attributed to the decrease in grain boundary and reduction in crystal system deformations which signifies increase in degree of perfection of grains with the removal of defects and healing of pores as a result of less number of grain boundaries, decrease in defects density and decrease in donor sites trapped at the dislocation and grain boundaries. Furthermore, crystallites ranges in size from small to large and crystallites as a result the smallest crystallite often possess the largest surface area to volume ratio such that given the higher surface area, they are more likely to be fragmented with annealing thereby enhancing crystal growth.

SEM analysis

The scanning electron microscopy results/micrograph at magnification of 20000 x for the semiconductor channel layer is shown in Fig. 4.

The average grain size of the SnS thin film semiconductor channel layer was calculated using imageJ software [18] and the histogram of the grain distribution is given in Figure 5. Otsu's thresholding method and particle analysis [19] was used after which statistical analysis of the data was made with histogram generated to study the grain distribution and

average grain size determined from the average particle size assuming round particles as confirmed by the analysis. The particle analyser was configured in a size range of 0 nm^2 to infinity in other to allow for coverage of smaller particles.

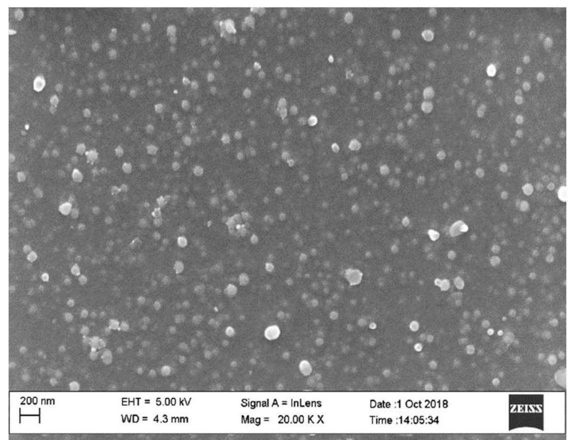


Fig. 4. SEM micrograph of the SnS semiconductor channel layer

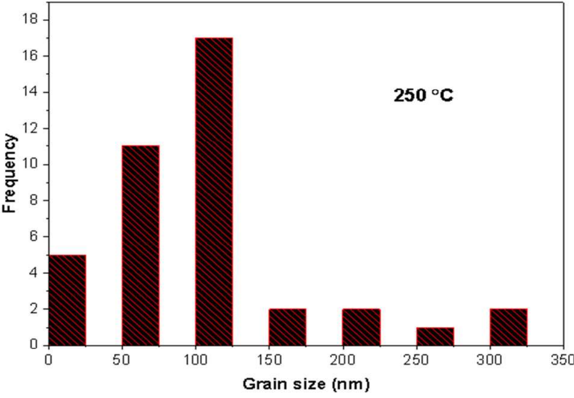


Fig. 5. Grain size histogram plot for SnS semiconductor channel layer annealed at 250 °C annealing temperature

The average grain size was found to be 137.53 nm. The histogram shows a non-uniform grain concentration and distribution at grain size range of 0.0 to 100 nm for the samples. The grain size distribution at 0.0 to 100 nm is larger than that of 100 to 350 nm range. There tends to be a preferred grain distribution and growth defining factor at 100 nm for all the samples which could be related to the preferred crystal orientation earlier defined by the XRD results. The increase in grain distribution from 0 to 100 nm range is followed by a decrease from 100 to 350 nm in all samples which could be attributed to initialisation of grain stability and uniformity at the range of 100 to 350 nm. The closely packed nature of the grains to each other reveals good adhesiveness of the deposited SnS thin film to the glass substrate. The larger grain sizes could enhance reduction in grain boundaries and potential barrier there by releasing charge carriers that were trap so as to further enhance carrier conductivity.

Temperature dependence of electrical conductivity

The temperature dependence of electrical conductivity of the deposited SnS thin film was studied by heating to a temperature of 300 °C after which the resistivity/conductivity was measured as the temperature reduced by 5 °C intervals. The obtained data was analysed using Arrhenius equation [20]. A plot of ln (σ/σ_0) versus (1/T) is given in Fig. 6.

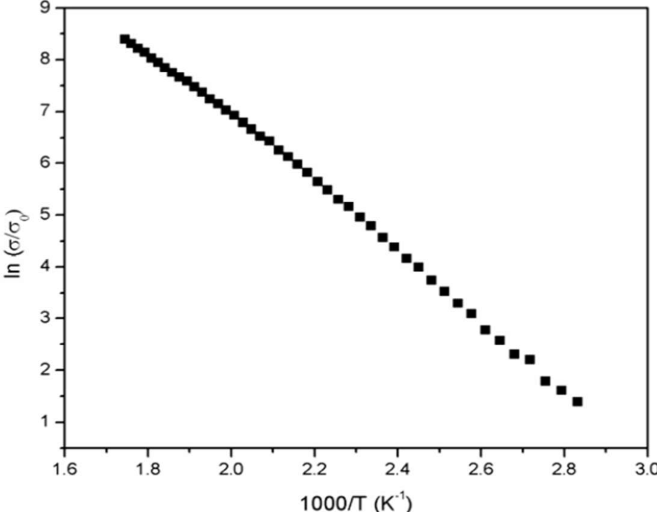


Fig. 6: The dependence of ln (σ/σ_0) versus (1000/T) for SnS thin film

The average activation energy of the charge carriers evaluated from the slope of the curve was obtained as 0.520 eV. The value of the activation energy could be attributed to the deep acceptor states stemming from the Sn Vacancy which plays significant role in p type carrier conductivity of the SnS semiconductor. The excess of Sulpur which is also evident in the elemental composition of the film, induces a proportionate Sn vacancy sites such that every anion would introduce

two positive type (p-type) conductor which is supported by the fact that the activation energy of the SnS thin film depends on elemental ratio, presence of crystal defect and the deposition method used. The SnS film conductance was observed to increase with temperature which indicates the semiconducting behaviour of the thin film. The excitation of charge carrier from valence band to conduction band could be responsible for the rise of conductivity [14].

Hall effect measurement for the SnS semiconductor channel layer

The measured electrical parameters of the SnS semiconductor channel layer from the Hall Effect measurement are given in Table 4.

Table 4.

Hall effect electrical parameters for the SnS semiconductor channel layer

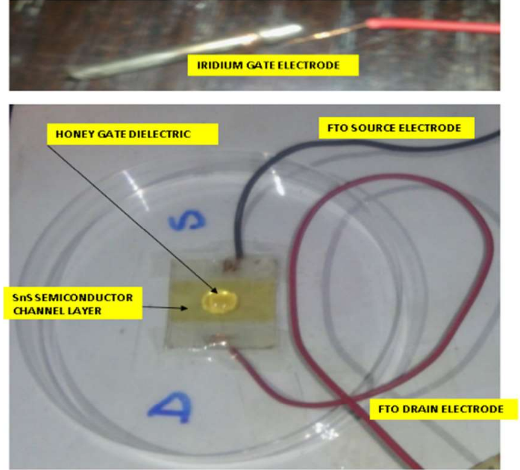
Annealing Temperature (°C)	Bulk concentration N_b (cm^{-3})	Average Hall coefficient R_H (cm^3/c)	Carrier mobility µ (cm^2/Vs)	Resistivity ρ (Ωcm)	Conductivity σ (Ωcm)$^{-1}$
250	3.167×10^{10}	1.971×10^{10}	1.619×10^{5}	1.025×10^{4}	9.756×10^{-5}

From Table 4, the average hall coefficient of the annealed SnS semiconductor channel layer is positive which indicates that the semiconductor channel layer is of p type carrier conduction with holes as majority carriers. Annealing increases carrier concentration, reduce resistivity due to improvement in crystallisation, greater grain size with annealing lead to decrease in defects density and crystal boundary which reduces resistivity hence increasing conductivity. This could be explained by the fact that annealing leads to improved crystallisation and increase in grain size in the films which could enhance the decrease of crystal defects and crystal bonding reduction, hence the release of trap electron and decrease resistivity [20].

The SnS EDLFET assembly

Fig. 7. shows a picture of the assembled SnS semiconductor channel layer Electric double layer field effect transistor with Honey gate dielectric. The measured gate capacitance of honey using LCR meter is 2.15 µF/ cm^2 while the dielectric constant is 20.50. Honey was used as a gel like electrolytic gate dielectric to generate an enhanced electric field response over SnS semiconductor channel layer. Due to the polarizability of honey, a diffusion of charge is formed at the thin layer between SnS semiconductor channel and honey. The thin layer forms an electric double layer which is a basic characteristics of ionic liguids contact with conductive materials and is as shown in Fig. 8.

A large charge gradient is formed on the surface of the SnS layer due to the nanoscale separation distance of the electric double layer. Application of positive gate voltage will cause the gate electrode to be positively charged such that when it is submerged in honey, anions accumulate at the gate/honey interface and cations at the honey/SnS interface. The electric double layer form at the honey/SnS interface alters the SnS semiconductor channel layer conductivity. Increase in positive V_{GS} will deplete the SnS channel of its free holes thereby turning it off.



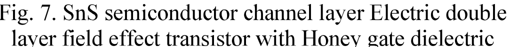


Fig. 7. SnS semiconductor channel layer Electric double layer field effect transistor with Honey gate dielectric

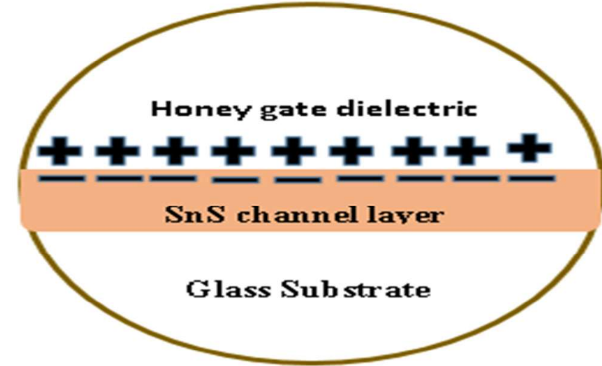


Fig. 8. Representation of charge distribution in honey/ SnS layer interface

Transfer and output characteristics of SnS EDLFET

Fig. 9. shows the transfer characteristics (Source drain current I_{DS} as a function of gate bias V_G) of the SnS EDLFET gated by honey dielectric at room temperature. While Fig. 10. Shows the output characteristics of the SnS honey gated EDLFET. The channel length for the device is 70 µm while the channel width is 4 mm.

At all values of the Vg used the gate current Ig≤ 10^{-3}Ids which signify that the fabricated device operates as a field effect transistor and specifically an electric double layer field effect transistor. From Figure 9, it is evident that the SnS EDLFET is a P channel device since the channel conductivity decreases with increasing positive gate bias. The I_{DS} increased with decreased in V_{GS} scanning which indicates a typical p-type transistor operation in the device. The device also operates in depletion mode, i.e. appreciable drain current flows at zero gate voltage as evident from the V_{GS}=0V drain current which is judged from the zero bias current in the transfer curve. The SnS EDLFET worked in a depletion mode with a normally "ON" state (i.e conducting without the application of gate bias voltage) which could be attributed to the maximum current flow from the source to drain when no difference in voltage exist between the gate and source electrodes.

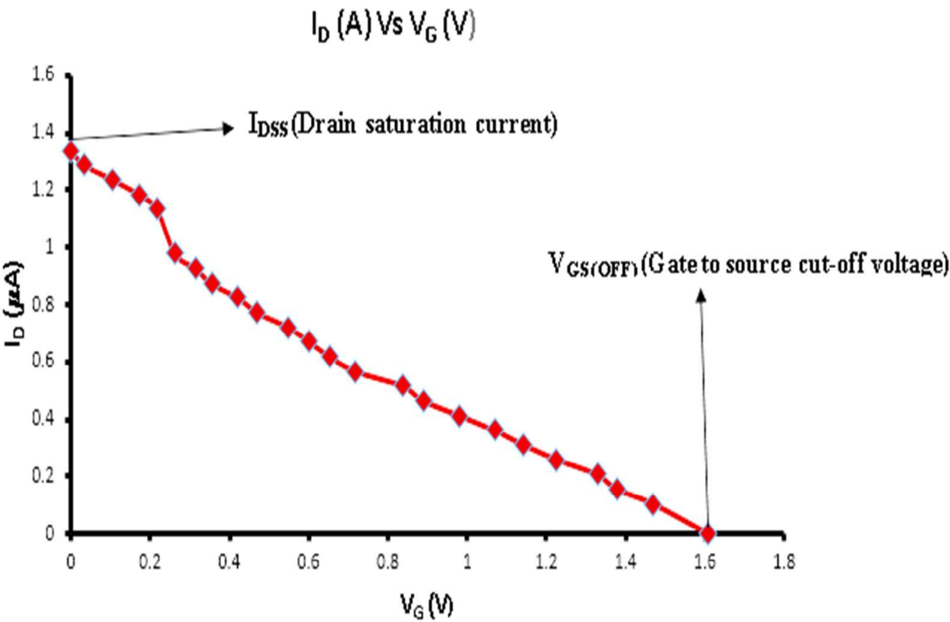


Fig. 9. Transfer curve of SnS honey gated EDLFET

The drain saturation current I_{DSS} as determined from the transfer curve at zero gate to source voltage (V_{GS}=0) and an applied drain to source constant voltage of 3V is 1.35 μA. This gives the maximum limiting current that can flow between the drain and source at V_{GS}=0. The drain current was observed to increase linearly then began to pinch off at the knee of the transfer curve at I_{DSS}. The I_{DSS} is temperature dependent with a negative temperature coefficient of approximately -0.5/°C. However with further application of gate voltage (positive V_{GS} than ($V_{GS\,(0ff)}$), the drain source channel could become more resistive by the changing size of the depletion region under the gate area such that the transistor is completely shuts off due to the depletion or shutting off of the majority charge carriers in the semiconductor channel.

From the transfer curve, the gate to source cut off voltage ($V_{GS\,(0ff)}$) was found to be 1.6 V which is the fundamental characteristics specifying the voltage necessary to turn the transistor device off. The gate to source voltage for a p channel device ranges from 0v for full conduction to several positive volts to turn it off. The 1.6V positive V_{GS} (less holes and less current) will deplete the SnS channel of its free holes thereby turning it "off". The low $V_{GS\,(0ff)}$ could enhance the choice off circuit design parameters. $V_{GS\,(0ff)}$ shifts with temperature and has a negative temperature coefficient of approximately -2mV/°C.

The transconductance which gives the amplifying factor of the transistor was obtained from the slope of the transfer characteristics as -809.61nA/V. The voltage required to increase the drain current by a factor of 10 which is also called sub-threshold slope (S) was estimated to be -1.6 $Vdec^{-1}$ from the curve of Log (I_D) versus $V_{GS.}$ It could be attributed to the presence of small carrier traps in the SnS thin film which might not necessarily include the grain boundary and is suitable for the switching of devices in active matrix flat panel displays.

The field effect mobility obtained from the transconductance is 16.67 cm^2/v at low V_{DS}. The mobility value implies more carriers passing through the channel per unit time which is essential for a FET and has the advantage of enhancing higher screen luminance.

Fig. 10 shows the output characteristics (I_D-V_{DS}) of the SnS EDLFET transistor measured at gate voltage (V_G) of 0.2 to 0.8 V with a 0.2 v scan which also supports the field effect transistor operation. No appreciable hysteresis was observed in the output characteristics, indicating that the channel is stable once it is formed. The I_D curves are flat at low V_{DS} indicating that a condition of hard saturation is achieved due to complete pinch off of the channel. No clockwise hysteresis

was observed which could be attributed to the non-availability or absence of continuous filling of traps by accumulated channel holes as V_{DS} is first increased from zero to a maximum of 0.8 V, then decrease back to 0 V. The fact that the I_D-V_{DS} characteristics curve do not show counter clockwise hysteresis indicates that ionic drift is not significant.

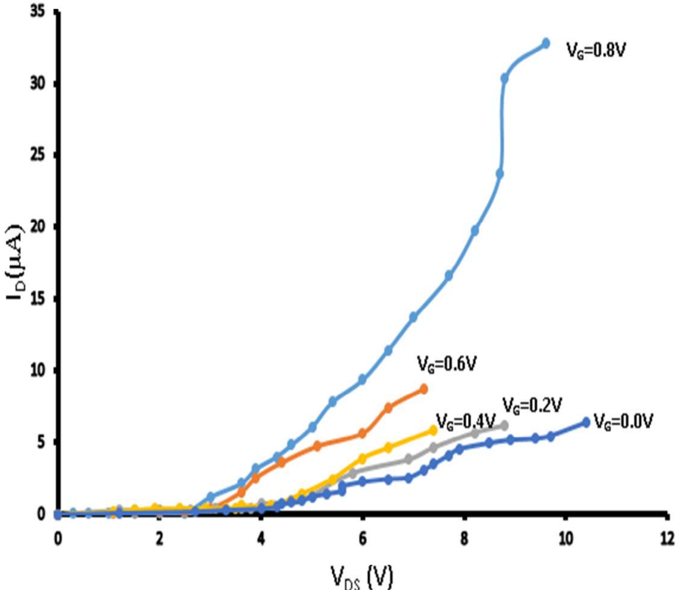


Fig. 10. Output curve of SnS honey gated EDLFET

CONCLUSION

The Electric double layer field effect transistor was assembled using tin sulphide (SnS) thin film whose thickness and annealing temperature were earlier optimised as semiconductor channel layer and honey as gate dielectric. The semiconductor layer was deposited using Aerosol assisted chemical vapour deposition (AACV) and annealed in open air at 250℃ on an etched region about the middle of a 4×4 mm FTO glass substrate with the source and drain electrode region defined by the etching and masking at the two ends of the substrate. Iridium was used the gate electrode while a copper wire was masked to the source and drain region to create contact. The thicknesses of the SnS layer was measured using profilometry, X-ray diffraction was used for phase and crystalline orientation, Scanning electron microscope was used to study the film morphology, the elemental composition of the film was determined by an Energy dispersive X-ray spectroscopy, Hall effect measurement and digital multimeters were a used to determine the SnS conductivity type, conductivity and the transistor characteristics. The SnS thin film was found to be polycrystalline consisting of Sn and S elements with define grains and of 0.4 µm thickness.

The SnS EDLT using honey as gate dielectric operated as p type channel in depletion mode with I_{DS} of 1.35 µA, $V_{GS\ (Off)}$ = 1.6 v, Trans conductance of -0.80961 µA/v, field effect mobility of 16.67 cm^2/v and sub-threshold slope of 1.6 $vdec^{-1}$ which are applicable as load resistors in synaptic transistor network, biosensor, logic gate circuits and in depletion load logic circuits. RF 9640, B15P are popular p channel depletion mode transistors in use.

Conclusively, very scanty reports have been made or exist on the study of SnS thin film applied to electronics as a semiconductor channel layer. SnS EDLFET using honey as gate dielectric offers an opportunity for further research and innovation into other materials that are unconventional in the expectation discovering new semiconductor and dielectric materials that are readily available and non-toxic. To the best of our knowledge and within the limit of available literature, no SnS based EDLFET has been reported hence making the results described here innovative to the scientific community.

Declaration of interest none.

ACKNOWLEDGEMENTS

This research did not receive any specific grant from funding agencies in the public, commercial, or not-for-profit sectors, However, the authors acknowledged the Staff and management of Alex Ekwueme Federal University Ndufu Alike Ikwo, Ebonyi state, Federal University of Technology Minna, Sheda Science and Technology (SHESTCO), Namiroch research laboratory Abuja, iThemba Laboratory South Afica and the electron microscopy unit of the University of Western Cape, South Africa for their various contributions.

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ЕЛЕКТРИЧНИЙ ДВОШАРОВИЙ ПОЛЬОВИЙ ТРАНЗИСТОР З ВИКОРИСТАННЯМ ТОНКОЇ SnS ПЛІВКИ В ЯКОСТІ НАПІВПРОВІДНИКОВОГО КАНАЛУ, А ТАКОЖ ДІЕЛЕКТРИЧНОГО ЗАТВОРУ З МЕДУ

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Дослідження було спрямоване на вивчення і застосування тонкої плівки SnS в якості напівпровідникового канального шару в збірці електричного двошарового польового транзистора, що має велике значення для успішної розробки нових концепцій пристрою, застосувань і зміни фізичних властивостей матеріалів, оскільки описані на сьогодні EDLFET (електричний двошаровий польовий транзистор) і модуляція електронних станів були реалізовані на оксидах, нітриді, вуглецевих нанотрубках і органічних напівпровідниках, при цьому рідко згадувались халькогеніди. Мед використовувався в якості гелеподібного електролітичного діелектричного затвора для підвищення рівня генерування відгуку електричного поля через шар напівпровідникового каналу SnS завдяки його здатності забезпечувати роботу при високому струмі і низькій напрузі за рахунок формування іонного гелеподібного розчину, подібного іонним гелям, які містять іонні рідини. Електричний двошаровий польовий транзистор був зібраний з використанням тонкої плівки сульфіду олова (SnS) як шару напівпровідникового каналу, та меду як діелектрика. Виміряна за допомогою LCR-вимірювача ємність медового затвору склала 2,15 мкФ/см^2, тоді як діелектрична константа – 20,50. Напівпровідниковий шар наносили за допомогою хімічного осадження з парової фази за допомогою аерозолю і відпалювали на відкритому повітрі при 250° C у протравленій області приблизно на середині скляної підкладки 4×4 мм з FTO покриттям, при цьому область електрода на джерельному і стічному електроді обмежувалася травленням і маскувавнням на обох кінцях підкладки. Іридій був використаний в якості електрода затвору, тоді як мідний дріт був замаскований у джерельній та стічній області для створення контакту з електродом. Для визначення характеристик пристрою були використані профілометри, рентгенівська дифракція, скануючий електронний мікроскоп, метод енергодисперсійної рентгенівської спектроскопії, вимір ефекту Холла та цифрові мультиметри. Було виявлено, що тонка плівка SnS є полікристалічною, такою, що складається з елементів Sn і S з дрібними зернами, з оптичним діапазоном 1,42 еВ і товщиною 0,4 мкм. Транзистор працював у режимі провідності каналу p-типу в режимі збіднення з мінливістю польового ефекту - 16,67 см^2/Vs, напругою відсікання - 1,6 V, струмом насичення зливу - 1,35 μA, коефіцієнтом трансдуктівності - 809,61 nA/V та підпороговим значенням нахилу - 1,6 Vdec^{-1}, що можна порівняти зі стандартними технічними характеристиками в електрониці. Позитивне зміщення затвора призводить до зрушення напруги відключення через захоплення заряду на межі поділу канал/діелектрик.

КЛЮЧОВІ СЛОВА: тонка плівка SnS, польовий транзистор, мед, електричний подвійний шар, напівпровідник