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Design, Construction And Characterisation Of Thirty- Two Output Multiple Pattern Moving Display System

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Abstract: A thirty-two output multiple pattern moving display system using discrete components was designed, constructed and characterized in this research work. The system comprises system clock, decimal counter, pattern logic gates, scanning clock, blink clock, pattern/output register, moving display load drivers and moving display load. The system clock is an astable multivibrator synthesized with 555 timer operating at a period of 12.5 seconds. The decimal counter (4017 counter I.C.) counts from state 0 to 9; ten distinct states. Now as it counts, the pattern logic gates designed with two 4000 logic chips (known as quad – 3 – input NOR gate with inverter) does some reasoning and decides which pattern to be displayed. The moving display-scanning clock, which is also, a free running multivibrator was designed to operate on two frequencies; a spelling frequency of 2Hz and a clearing frequency of 1kHz. The output registers are five 74164 shift registers I.Cs. They are loaded high by the pattern register- another 74164, whenever a pattern is to be displayed and loaded low during clearing mode. During the blink mode, the blink clock, which is another free running multivibrator designed to operate at a period of 2 seconds is activated. The output of blink clock is applied to the reset terminals of the whole system registers and therefore the registers are reset every 2 seconds putting the whole system off and on. All the registers together feed the load drivers; thyristors (BT 151-500R) and the loads are small ac voltage bulbs used to illuminate permanently fixed letters to indicate their presence. There are all together five patterns of display. The system has been successfully tested and it worked.

Introduction

A display means an opto - electronic device that can show a number ("numeric" display); a hexadecimal digit, namely 0 – 9 and A – F ("hexadecimal display"), or any letter or number ("alphanumeric display"). The dominant display technologies today are Light Emitting Diodes (LEDs), and Liquid Crystal Displays (LCDs). These replaced the small incandescent lamps which used to be standard for front – panel indicators (Horowitz and Hill, 1995).

LEDs behave electrically like ordinary diodes, but with a forward voltage drop in the range of 1.5 to 2.5 volts. When current, typically 5mA to 20mA flows in the forward direction, they light up and produces adequate brightness. LEDs are cheaper than incandescent lamps, they last almost forever, and they are even available in three colours (red, yellow and green) (Ryder, 1979; Ahmed and Spreadbury, 1978; Faissher, 1991; Horowitz and Hill 1995).

LCDs are the newer technology, with significant advantages for:

(a) Battery operated equipment, owing to its very low power dissipation.
(b) Equipment for use outdoors or in high ambient light levels.
(c) Displays that require custom shapes and symbols and
(d) Displays with many digits or characters. LEDs, by comparison, are somewhat simpler to use, particularly if one only need a few digit or characters.

They also look good in subdued light, where their good contrast make them easier to read than LCD displays (Horowitz and Hill, 1995; Mehta and Mehta, 2004; Tokheim, 2004; Sclater, 1999; Ali, 1998; Theraja, 1982).

For displays of many characters – say a line or two of text – gas discharge ("plasma") display panels compete with LCDs particularly if one care about clarity and contrast. They do require significant power, however, so LCD displays are usually preferred for battery – power

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application (Tokheim,2004; Faissher,1991; Ryder,1979; Ahmed and Spreadbury,1978; Horowitz and Hill,1995).

This project makes use of small alternating voltage bulbs of about 15 watts each operating on 220/230VAC mains to light up permanent fixed letter on the sign board.

Science could be defined as knowledge as of facts, phenomena, laws, and proximate causes, gained and verified by exact observation, organized experiment and analysis. Technology, which is applied science is the sum total of the technical means employed to meet the material needs of a society. It then follows naturally that science and technological advancement is systematic and sequential: sequential in the sense that advancement to the next level or stage is an improvement of the preceding stage(s). And improvement is dependent on the level of understanding of the previous level or stage; nature abhors a vacuum.

Science and technological advancement in the world, now a global village, is lopsided with the developing countries, like Nigeria lagging the developed world of western countries. This poses a great challenge to the former because in trying to catch up with trend of science and technological advancement, the developing world like ours tends to jump stages of the development which are crucial to successful technological advancement. It is pertinent to note that the leading industrialised nations of the world never jumped stage(s) but started earlier in time and sequentially passed through the stages of technological advancement and improving on them over the years.

Hence if we must be like them we must brace up to the challenges and embrace stages of technological advancement.

Electronic circuit design process is where a current and or a voltage may be specified and the elements required to establish the designated levels must be determined. This synthesis process requires a clear understanding of the characteristics of the device, the basic equation for the network, and a firm understanding of the basic laws of circuit analysis. The design sequence is obviously sensitive to components that are already specified in terms of electrical parameters (Randyslone, 2001).

The success or failure of electronic circuit design depends, to a very large extent, on how well these electrical parameters or characteristics are met. The reliability, durability and dependability of the system also depend on this. And these device parameters are specified in the micro electronics industry, which is the branch of electronics that deals with electronic components manufacturing. Therefore micro electronics is where the action is.

Micro electronics technology has advanced so rapidly in recent years that we now have complete electronic systems like radio, microprocessor etc on a single chip as a result of large scale integration (LSI) and Very Large Scale Integration (VLSI) (Horowitz and Hill,1995). In fact the rate of growth in the industry poses a very great challenge to developing countries like ours, so much so that in our bid to catch up with the trend we tend to jump stages; this is the worst thing to do.

Most display systems in our institutions, organizations or departmental stores like Mr Biggs are based on microprocessor – a result of VLSI.

This multiple pattern moving display system was successfully designed and implemented with discrete components and as such it demonstrates an unavoidable step or stage towards technological advancement in the microelectronics industry.

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Descriptions of Components

The Transistor BC 107

This is a bipolar NPN transistor; it is used as a switch at different points in the circuit.

The Integrated Circuits (ICs)

There are several types used according to their individual functions. They are as follows:

a. L M 7806. It is a three terminal (input, output and ground) voltage regulator that is factory trimmed to provide a fixed output. The voltage is specified by the last two digits of the part number (Floyed, 2002; Boylestad and Nashelsky, 2002; Tokheim, 2004; Horowitz and Hill,1995).

b. NE 555 timer IC: as the name implies it is used to generate waveform as relaxation oscillator. Its structure is shown in Fig. 1 below:

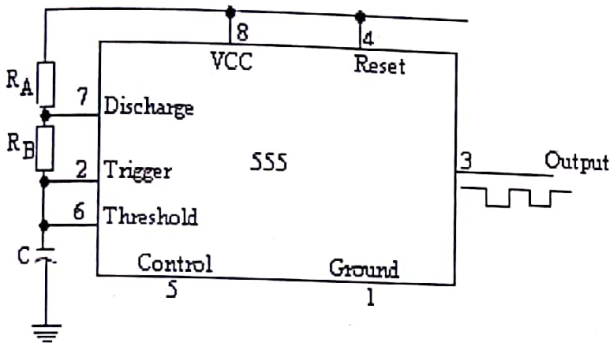

Fig. 1. The 555 Pin Out Structure Connected as an Oscillator.

The output goes high (near Vcc) when the 555 recieves a trigger input and it stays there until the threshold input is driven, at which time the output goes low (near ground) and the discharge transistor is turn on. The trigger input is activated by an input level below 1/3 Vcc. (Morant,1990; Ali,1998; Jacobwitz, 1976; Bartelt,1997).

When power is applied, the capacitor is discharged; so the 555 is triggered, causing the output to go high, the discharged transistor Q1 (in built) to turn off, and the capacitor to begin charging towards Vcc through RA + RB. When it reached 2/3 Vcc, the threshold input is triggered, causing the output to go low and Q1 to turn on, discharging C toward ground through RB. Operation is now cycling, with C's voltage going between 1/3 Vcc and 2/3 Vcc, with period T= 0.693 (RA + 2RB). The output generally used is the square wave output. The 555 makes a respectable oscillator with stability approaching 1%. It can run from a single positive supply of 4.5 to 16 volts, maintaining good frequency stability with supply voltage variation because the threshold tracks the supply fluctuations. (Morant,1990; Horowitz and Hill,1995; Boylestad and Nashelsky,2002).

c. 4017 counter I C: this is a BCD (Binary Coded Decimal) decade counter with decoded 1 – of – 10 outputs. It is a 5 bit (binary digit) with synchronous clocking system; all clock input count on positive edge clocking, asynchronous reset; all reset input count on negative edge, count down only. (Floyed, 2002; Sclater, 1999; Charles, 1978).

d. 4000 logic chip: this is called logic chip because it does some reasoning and decides whether or not to open its gate (output) depending on the logic levels at the input (Millman and Halkias, 1972; Morant, 1990; Floyed, 2002; Sclater, 1999; Charles,1978). The schematic and pin out is shown in Fig. 2 below

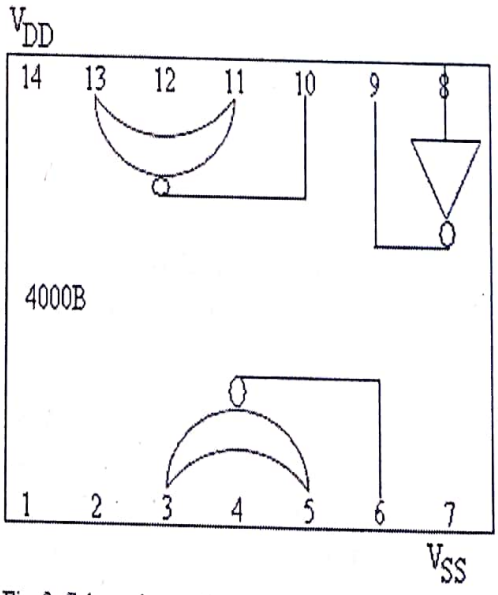

Fig. 2: Schematic and Pin Out of CD4000B

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e. 74164 shift register I C: registers are used basically to "hold" data (a set of bits). A set of D flip-flop constitutes a register but the separate clocks, or set and clear inputs are tied together. Shift registers are made by connecting a series of D flip-flops so that each Q output drives the next D input, and all clock inputs are driven simultaneously. At each clock pulse the pattern of O's and I's in the register shifts to the right, with the data at first D input entering from left. (Horowitz and Hill,1995). Representation of D flip-flop is shown in Fig. 3 below.

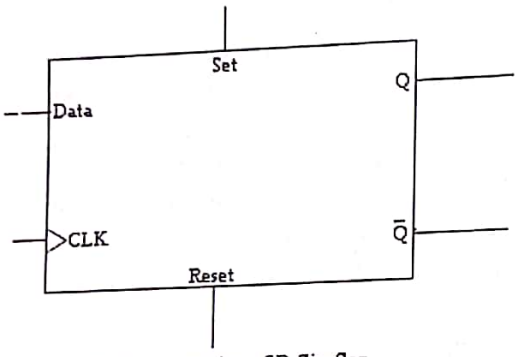

Fig. 3: Representation of D flip-flop

This particular shift register (74164) is 8 bit 14 DIP (dual in-line package) pin outs, 2 state serial input, parallel output (2-state totem pole), direction of shift is right and has asynchronous reset. (Floyed, 2002; Sclater, 1999;).

Design and Construction

The display system is configured in modular scheme. The modules are: power supply module, system clock module and display module.

Design of Power Supply Module

This system was built using integrated circuits (ICs) based on transistor-transistor logic (TTL) and complementary metal oxide semiconductor (CMOS) technologies. While the later has a wider supply voltage range of +3 to +15 volts, the former (TTL) has a supply voltage of 5V±5% (Horowitz and Hill, 1995; Millman and Halkias, 1972; Bishop et al, 1994;Ryder, 1979; Ahmed and Spreadbury, 1978; Faissher, 1991). Bearing this in mind a supply voltage of +6 volts was chosen since it is compatible with both technologies. The power supply elements (components) include;

(a) Transformer,
(b) Filter capacitor
(c) Rectifier diodes and
(d) Six (6) volts voltage regulator IC

(a) The transformer : For a +6 volts regulator it is good to use an unregulated input of about +12 volts at the minimum of the ripple, which itself might be a volt or two (Horowitz and Hill, 1995; Millman and Halkias, 1972; Bishop et al, 1994;Ryder, 1979; Ahmed and Spreadbury, 1978; Faissher, 1991).The secondary voltage rating determines the d.c output from the bridge, since the peak voltage (at the top of the ripple) is approximately 1.4 times the r.m.s secondary voltage, less two diode drops. This is to be absolutely certain that the input to regulator will never drop below the minimum necessary for regulation, typically 2 to 3volts above the regulated output voltage, else one may encounter 100Hz in the regulated output.

(b) Filter capacitor: is chosen large enough to provide acceptable low ripple voltage, with voltage rating sufficient to handle the worst case combination of no load and high line voltage (240-260r.m.s).For the +6 volts, 1 amp regulated supply, contending with a ± 10% worst case line voltage variation, it is ideal to keep ripple to less than 2 volts peak to peak (pp). (Horowitz and Hill, 1995; Tokheim, 2004; Mehta and Mehta, 2004; Theraja, 1982; Ali, 1998):

$$\frac{dV}{dt} = \frac{1}{C} \qquad 1$$

where V is the Voltage applied to the Capacitor and C is the capacitance of the Capacitor

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$$Peak-to-Peak\ ripple = \frac{IT}{C} \quad 2$$

$$T = period = \frac{1}{f}$$

$f = frequency = 50Hz$

$C = capacitor\ value$

$I = current = 1amp$

For bridge rectifier (Because the negative part of the sinusoids is taken into account)

$$= 2x50Hz = 100Hz$$

$$\text{Therefore, } T = \frac{1}{100} = 0.01s$$

For 2 volts pp,

$$2 = T\frac{dV}{dt} = \frac{IT}{C}$$

$$2 = 0.01x\frac{1.0}{C}$$

$$C = \frac{0.01x1.0}{2}$$

$$C = 5000\mu F$$

In choosing capacitor value, 20 % tolerance is always allowed. An oversize capacitor not only wastes space but also increases transformer heating by reducing the conduction angle. Therefore 4000uF, 25V is a minimum size choice (Horowitz and Hill, 1995; Bartelt, 1997; Boylesstad and Nashelsky, 2002; Theraja, 1982)

(c) Diode rectifier: Typical of rectifier is the popular IN 4001- IN 4007 Series, rated at 1 amp, with reverse breakdown voltage ranging from 50 to 1000 volts. Full wave rectification is better in this respect, since a greater portion of the transformer waveform is used. (Horowitz and Hill, 1995; Floyed, 2002; Sclater, 1999).

(d) 7806 IC regulator ; is chosen because it can provide up to 1amp load current and has on- chip circuiting to prevent damage in the event of overheating or excessive load current; the chip simply shuts down, rather than blowing out (Floyed, 2002; Horowitz and Hill, 1995). The power supply module circuit diagram is shown in Fig. 4 below.

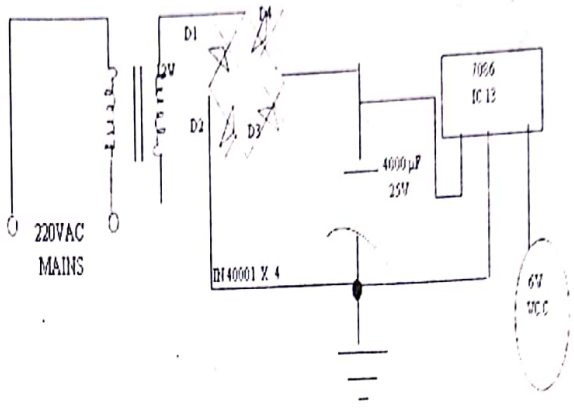

Fig 4: Power Supply Module

Design of System clock Module

System Clock: This is an astable multivibrator operating on 6V and a period of 12.5 seconds. Therefore 555 timer can perform the function. For a 555 timer as an astable muitivibrator, the operating period equation is:

$$T = 0.6939(R_1 + 2R_2)C_T$$

(Ali, 1998; Tokheim, 2004; Joseph and John, 1968; Theraja, 1982; Horowitz andHill, 1995; Boylestad and Nashelky. 2002)

Where R1 and R2 are timing resistor and CT is timing capacitor

For the system clock (IC 10)

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$R_1 = R_5$

$R_2 = R_6$

$C_T = C_5$

$T = 12.5secs$

Putting $R_5 = 2.2m, R_6 = 1.2k$

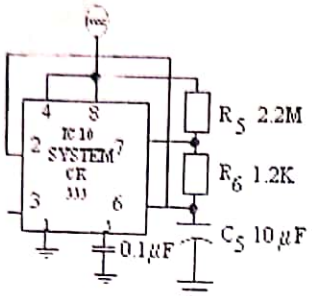

Fig 5 System Clock

Using the values in equation (1.3)

$12.5 = 0.693\{2.2x10^6 + 2(1.2x10^3)\}C_5$

$= 1.525x10^6 C_5$

$C_5 = \dfrac{12.5}{1.2526x10^6}$

$= 8.19x10^{-6}$

$C_5 \approx 10\mu F$

Moving Display Scanning Clock: This is also a free running multivibrator synthesized with 555 timer By Eq. 3

Scanning period $T = 0.693(R_1 + 2R_2)C_T$

$T = 0.5sec$

$R_1 = 12k$

$R = 1.2k$

$C_T = C_1$

Therefore, $T = 0.693(12x10^3 + 2x1.2x10^3)C_1$

$= 9979.2C_1$

$C_1 = 5.01x10^{-5}$

$C_1 = 50\mu F \approx 47\mu F$

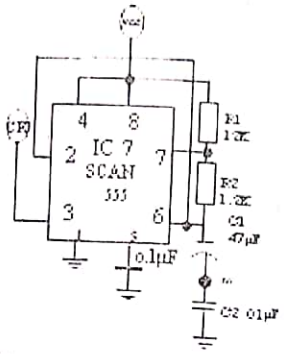

Fig.6: Scanning Clock

During clearing mode C_1 will be in series with C_2

Therefore, $C_T = \dfrac{C_1C_2}{C_1 + C_2}$ (Ali, 1998; Boylesta and Nashelsky, Sclater, 1999)

With a clearing frequency of 1kHz clearing period is therefore 0.001

Therefore, $0.001 = (0.693(R_1 + 2R_2)\dfrac{C_1C_2}{C_1 + C_2}$

$0.001 = (0.693(12x10^3 + 2x1.2x10^3)\dfrac{C_1C_2}{C_1 + C_2}$

$1.002x10^{-7} = \dfrac{C_1C_2}{C_1 + C_2}$

$C_1C_2 = 1.002x10^{-7}C_1 + 1.002x10^{-7}C_2$

But $C_1 = 47\mu F$

$47x10^{-6}C_2 = 1.002x10^{-7}x47x10^{-6} + 1.002x10^{-7}$

$4.6899x10^{-5}C_2 = 4.70994x10^{-12}$

$C_2 = 1.004x10^{-7}\mu F$

$C_2 = 0.1\mu F$

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Blink clock-: This is an astable multivibrator with a period of two seconds. Using Eq. 3

$$T = 0.693(R_1 + 2R_2)C_T$$

$$R_1 = R_3$$

Here $R_2 = R_4$

$$C_T = C_4$$

Putting $R_3 = R_1 = 20k$, $T = 2\sec s$

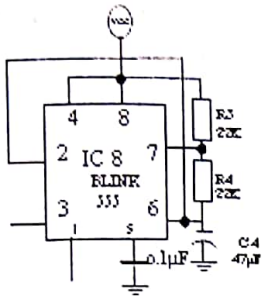

Fig.7: Blinking Clock

Therefore $2 = 0.692(20x10^3 + 40x10^3)C_4$

$$= 41580C_4$$

$$C_4 = \frac{2}{41580}$$

$$C_4 = 48\mu F \approx 47\mu F$$

2.03 Design of Display Module: This consist of the output registers TTL 74164 series. series of power switching thyristor type BT 151 series as shown in Fig. 8.

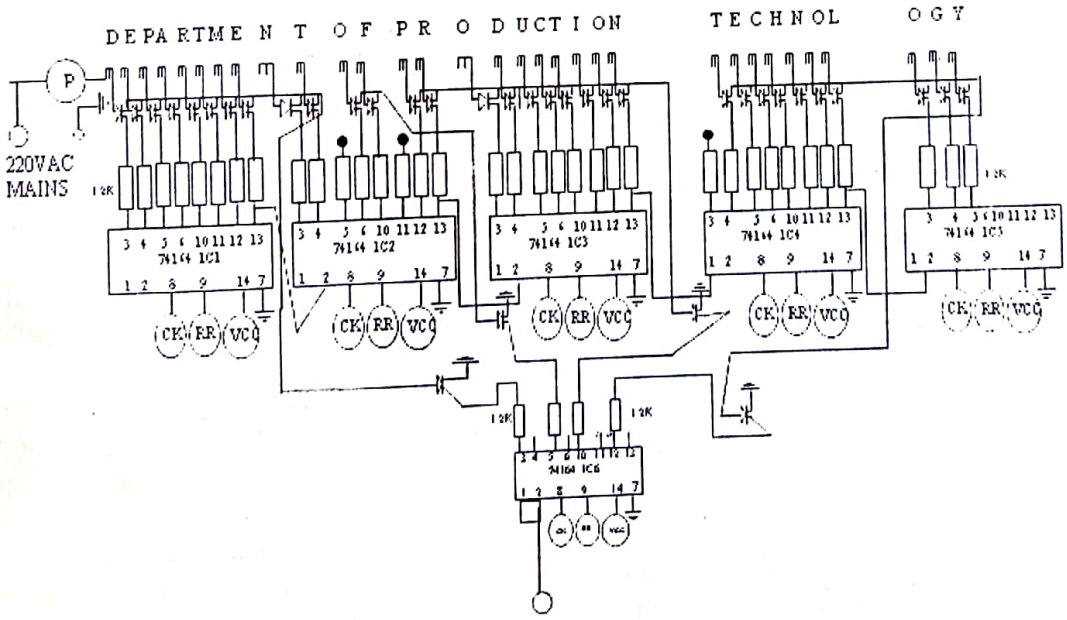

Fig.8 Display Module

Result and Discussion

System Operation and Pattern Generation

The arrangement of the thirty two-letter inscriptions on a signboard is shown in Fig. 9. The circuit diagram of the complete system is shown in appendix. The operation is such that when the system is put on it will sequentially spell the letters from beginning to the end. At the end of each word it pauses for about two seconds, indicating the end of the word before continuing with the next word. Whenever each letter is lit it remains on until that particular pattern is over. At the end of the pattern all the letters will remain conspicuously lit and displayed completely for an observer to interpret. When the last letter in the inscription is lit, the whole system stays on for about five seconds before going off, thereby marking the end of the first pattern of the display. The second pattern commences with the words coming on in sequence, that is rather than spelling the inscription in letters it is spelt in words. After each word the system pauses for about one second before lighting the next word. When each word is spelt it remains on so that after the last word the whole inscription remains on once again for an observer to interpret completely. It remains on for about 8 seconds and goes off, again marking the end of the second pattern. In the third pattern the word-spelling mode continues and go off after about 12 seconds. The system is designed such that the whole words flashes on and off for about six times in its fourth pattern. In its fifth and final pattern, the whole inscription comes on at a go and remain on for about 12 seconds. At the end of this pattern the system is completely reset and the patterns commence all over again from the beginning.

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Fig. 9: The assembled electronic signboard.

Letter Spelling Mode: When the system is put on the system clock unit (IC 10), which is a free running multivibrator synthesized with 555 timer and operating at a period of 12.5 seconds, is automatically activated. Whether the clock output is low or high the pattern decimal counter (IC 9) has its decimal 'O' output which is on pin 1 high. All other decimal outputs of the counter are low. Output of gate 3 of the pattern logic chip (IC 12) is, by connection from the pattern decimal counter, high thereby providing one condition for the bottoming of the moving display scanning clock frequency selection transistor Q1.By connection from the pattern decimal counter output of gate 4 of the logic chip is high and inverted by the inverter, presenting the same transistor with a low condition at the emitter and the transistor therefore saturates. The junction m of the moving display scanning clock is accordingly grounded. This clock which is also activated on system switch on has two operating frequencies; a spelling frequency of 2Hz and a clearing frequency of 1kHz. As the junction m is grounded the frequency components in the circuit will be R1, R2 and C1 and hence the clock (Ic 7) scans the output registers (ICs 1,2,3,4 and 5) and the pattern register (IC 6) at a spelling frequency of 2Hz.

By connection from pattern decimal counter the output of the logic gate 2 of the logic chip (IC 11) is high. The data input (pins 1 and 2) of the pattern register are loaded high, ready for transmission to the register's outputs. The system is now said to be in letter-spelling mode. As the scanning

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clock runs, the output of the output registers go high from left to right. The last output of the first register enables the second register which does the same to the third register which does the same to the fourth register and so on till the last output of the last register (IC 5). The outputs of the pattern register also go high from left to right. All the registers together feed the load drivers. The load and rhe drivers shall be considered later.

When the first pulse from the system clock comes the decimal output '1' (pin 5) of the decimal pattern counter goes high and the system still remains in the letter spelling mode. The first two decimal outputs are allowed to control the first pattern spelling mode because the system clock period is not enough to accommodate the time it will take to spell the whole letters and the period cannot be increased further to avoid undue of time length when the pattern register data is cleared after each pattern. The pauses after each word occur by floating one other following terminals after each word.

When the clock seconds pulse comes the decimal output '2' (pin 6) of the counter is high. By connection gate 4 releases the emitter of Q1 and hence the junction 'm' is accordingly released from ground. Gate 2 loads in zero at the data inputs of the pattern register. The display scanning clock now runs at a clearing frequency of 1kHz.

Thus all the outputs of pattern register (IC 6) go low, putting the load off. The system is now in the first clearing mode (CL 1) and stays for 12.5 seconds as dictated by the clock, thereby marking the end of the first pattern.

First word spelling mode: The second pattern is spelling of the inscription in words. When the third pulse from the system clock comes, the decimal output '3' (pin 9) of the decimal counter goes high. As explained in the first pattern the junction m of the scanning clock is grounded and the clock once again runs at a scanning frequency of 2Hz. The data inputs of the pattern register again see logic high level. Remember that the contents of the output registers have not been cleared; only that of the pattern register. By connection individual words are permanently tied to the individual and corresponding output of the pattern register in sequence. Therefore as the scanning clock runs the words are put on in sequence because the coming on of any output from the pattern register puts a whole word on since the output register are still high at this stage . The pauses after each word are caused by floating a terminal after each word. After the last word the whole inscription stays on for 8.5 seconds.

When the fourth pulse comes the decimal output '4' of the pattern counter goes high and every other output of it is low. By connection the junction m is again released, causing the clock to run at a clearing frequency of 1kHz. The data inputs of the pattern register are also loaded low. As the scanning clock runs, the outputs of the pattern register quickly go low, putting the display off. This is the second clearing mode (CL2) of the system and that marks the end of second pattern.

Second word spelling mode: In this third pattern the system is designed to continue its word spelling mode as described in the preceding section.

After about 12 seconds the sixth pulse from the system clock comes and the decimal output '6' of the decimal counter rises high. The decimal output '5' returns low. For the moving display scanning clock to maintain a high clearing frequency of 1kHz the high decimal output '6' is now transmitted to gate 3 of logic chips and therefore its output goes low, rubbing Q1, of its base voltage and hence junction 'm' remains high. By connection the inputs of the pattern register again experience low logic level. As the scanning clock runs the

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pattern register outputs quickly go low, putting the display off and the system is said to be in the third clearing mode.

Blink Mode: In the fourth pattern the display blinks every 2 seconds for about 12.5 seconds. When the seven pulse from the system clock reaches the decimal pattern counter the decimal output '7' of the counter rises high. By connection, the junction 'm' of the display-scanning clock is still released. The data inputs of the pattern register are loaded high. The pattern register outputs now quickly go high. But the high decimal output is applied to the base of Q2, saturating it and this grounds pin 1 of the whole system blink clock (IC8). The blink clock is consequently activated to run at the period of 2 seconds. The output of blink clock is applied to the reset terminals of the whole system registers and therefore the registers are reset every two seconds putting the whole system off and on. When the pulse level is low the registers are reset because low- level condition at the reset terminals of these registers resets them. When the pulse level is high the register's reset terminals are released and the scanning clock quickly scans through the registers, putting the outputs high quickly and deceiving the eyes into seeing a one-time display.

Full Blast, and Reset Mode: On receipt of the eight pulse from the system clock, the decimal output "8" of the decimal counter goes high. Decimal output "7" now because low, disabling the blink clock and flashing ceases, in which case the whole inscription stays on steadily for about 12 seconds. At this juncture the moving display scanning clock still maintains a high frequency of 1kHz, but unlike the clearing mode, gate 2 of the pattern register logic chips loads high to the data inputs of the pattern register. The scanning clock therefore causes the data to quickly sweep through the register, deceiving the eyes into seeing the words coming on at a time because of the high frequency.

The system enters into the reset mode at the expiration of this pattern which occurs when the ninth clock pulse comes, causing the decimal output "9" to go high. The high state appears at the reset terminal of decimal counter thereby resetting it. The same high state appears at the base of the registers reset transistor Q3, saturating it and bringing the reset terminals of the registers low and hence resetting the whole registers. When the whole system is completely reset it starts all over again from the first pattern. Table 1. below helps to clarify the conditions of various units at various patterns.

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Table 1. Conditions of Various Units at Various Patterns

S/NO	System Clock	Moving display clock frequency	Output register's output	Pattern register output	Blink clock state	Decimal counter high output	Action
0	Zero pulse	2Hz	Go high in sequence	Go high in sequence	Inactive	'O'	Letter spelling mode (1S1)
1	First pulse	2Hz	Go high in sequence	Remain high	Inactive	'1'	Letter spelling mode (1S2)
2	Second pulse	1KHz	Remain high	Go low in sequence	Inactive	'2'	First clearing mode(CL2)
3	Third pulse	2Hz	Remain high	Go high in sequence	Inactive	'3'	Word spelling mode (2S)
4	Fourth pulse	Go high in sequence	Remain high	Go low in sequence	Inactive	'4'	Second clearing mode (CL2)
5	Fifth pulse	2KHz	Remain high	Go high in sequence	Inactive	'5'	Second Word spelling mode (3S)
6	Sixth pulse	1KHz	Go low in sequence	Go low in sequence	Inactive	'6'	Third clearing Mode (3S)
7	Seventh pulse	1KHz	Go low and high	Go low and high	Active and frequency of 0.5Hz	'7'	Blink mode (4S)
8	Eight pulse	1KHz	Go high in sequence	Go high in sequence	Inactive	'8'	Full blast mode (5S)
9	Nineth pulse	2Hz	Remain low	Remain low	Inactive	'9'	Reset mode (R)

Conclusion

In conclusion, the design and implementation of thirty-two out put multiple pattern moving display system was successful using discrete components and ICs. In depth understanding of the electrical characteristics of these components ensured the satisfactory and efficient performance of the system.

Since the feasibility of the product arising from this work has been demonstrated it is pertinent for developing countries like ours to establish indigenous microelectronics industry to enable us participate in the sequential advancement in technology rather than jumping to what the developed countries dumps on us. In so doing we will be able to fashion out customised technology that will suit our peculiar need. This will further develop and advance our indigenous technology and put us on the path of competition rather than dependence; dependence in this context is perpetual slavery.

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