Power Quality Improvement Using an Active Power Sharing Scheme in More Electric Aircraft

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***Abstract*—This paper proposed a harmonic suppression scheme that used a DC-DC converter as an active harmonic injector to cancel voltage harmonics on the HVDC bus within a hybrid power generation centre (HPGC). A permanent magnet synchronous generator and a battery are considered to supply power to a common HVDC bus through their dedicated AC-DC and DC-DC converters respectively within the HPGC. We proposed simplified mathematical models of harmonics from the AC-DC and DC-DC converters. Thereafter, an active power sharing scheme between the PMSG and the battery is developed to control the magnitudes of targeted harmonics to be the same. The targeted harmonics on the HVDC bus can thus be cancelled by properly tuning the carrier signal phase angles within AC-DC and DC-DC converters. A closed-loop control scheme has been developed and this scheme is with no extra hardware cost. To demonstrate the effectiveness of the proposed scheme, we selected the first-band harmonic (f_c-3f_0) as the targeted harmonic component. The harmonic cancellation scheme for this component has been developed and validated using experimental results. It has been demonstrated that the proposed method can achieve over 90% reduction of this specific harmonic component on the HVDC bus within this HPGC using one DC-DC converter.**

***Index Terms*- DC power generation, capacitors, harmonics, power sharing ratio.**

I. Introduction

To achieve more efficient and environmentally friendly solutions of travel, more electric aircraft (MEA) concept is one of the major trends towards future aerospace development [1][2]. Onboard MEA, pneumatic, hydraulic, and mechanical subsystems are replaced by their electrical equivalences, which results in a significant increase in power demand. To supply electrical loads onboard, the common dc bus architecture has received significant attention these days [3][4]. With the common dc bus architecture, electrical generators are supplying a DC bus through an AC-DC converter together with energy storage elements. As shown in Fig. 1, the DC bus is supplied by an electrical generator and a high-voltage battery through their dedicated converters. Also, a permanent magnet synchronous generator (PMSG) is used to extract electrical power from the high-speed engine shaft. An energy storage system (ESS) with a battery is integrated for the flexible operation of power flow. These two power sources, together with a high-voltage bus capacitor, form a hybrid power generation centre (HPGC), as shown in Fig. 1.

With such a structure, expected benefits include less need for cables, high flexibility of power management, and higher redundancy ability under fault conditions. The hybrid DC power generation system has been widely considered not only for the MEA but also for hybrid vehicle [5], ships [6] and microgrid [7].

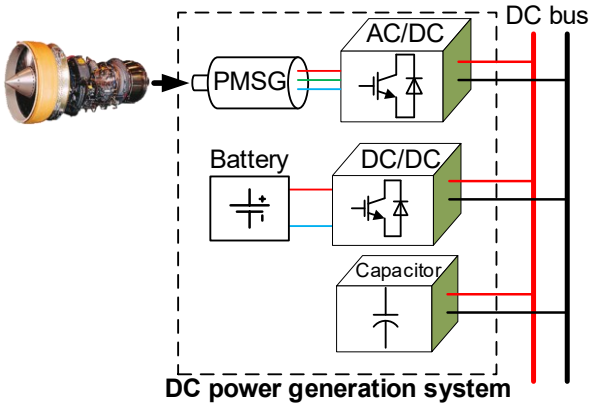

Fig. 1. Hybrid DC power generation system on MEA.

In the HPGC system shown in Fig. 1, the capacitor bank is used to filter out high-frequency fluctuated currents and flatten the DC-bus voltage, such that the DC-bus voltage meets the DO-160E [8] and MIL-STD-704F [9] standard. However, the capacitor is always bulky and expensive. With reduced harmonics, reduced size and weight of the dc-bus capacitor can be achieved. This, in return, gives the system a higher efficiency, reduced mass and lower fuel consumption. Furthermore, with lower harmonics, the capacitor lifetime is extended as well [10].

Active suppression methods have attracted more attention to suppressing harmonics on capacitors due to their flexibility and high performance. The fundamental idea of those methods is to adjust the switching actions of power converters to minimize

This work was supported by the Clean Sky 2 Joint Undertaking under Grant 807081. (Corresponding author: Tao Yang.) The author Cheng Wang also thanks the stipend funding from China Scholarship Council (CSC).

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the harmonics.

Adding an extra circuit is the most straightforward solution for reducing capacitor harmonics generated from switching frequencies [12]-[15]. This kind of methods can be implemented on all systems with power electronic devices. However, it requires extra elements and thus increases the cost and complexity of systems.

Some researchers have investigated harmonic suppression in the second switching frequency for the DC power system [16][17]. However, the first-band harmonics are not considered, which contributes more to DC-link fluctuation when the PMSG works under high modulation index [18]. In [19], the authors proposed a dynamic PWM interleaving method to suppress the first-band harmonic. However, as a side effect of this method, the AC harmonic current of PMSG deteriorates, which limits its application on MEA.

In this paper, we proposed a new power-sharing control scheme to achieve power sharing (between PMSG and the battery) and harmonic suppression at the same time. Through active power sharing, magnitudes of harmonic components from the AC-DC and DC-DC converters can be actively controlled. Controlling targeted harmonic components (f_c-3f_0 component studied in this paper) from the AC-DC and DC-DC converters of the same magnitudes, appropriate phase shifting between those harmonic components will enable the harmonic suppression and cancellation.

This paper is a follow-on research of our previous publication [16], where harmonics of two AC/DC power converters have been actively controlled with one AC-DC converter used as a harmonic sink. In this paper, we focus on using the DC-DC converter as an active harmonic damping device to suppress the first carrier sideband harmonic (f_c-3f_0 frequency harmonic component from one AC-DC converter). Although we select some specific harmonic components for suppression, the proposed method can essentially be used to suppressing any harmonic component of interest by simply changing the feed-back component.

The paper is organized in the following manner. Section II and III present basic mathematical analysis of switching harmonics generated from the AC-DC and DC-DC converters, respectively. Based on the mathematical models, Section IV illustrates an enhance harmonic suppression method by adjusting power sharing between PMSG and ESS system and actively tuning the phase-shift angle of the carrier signals. Section V gives the experiment results of the proposed method, and Section VI concludes this paper.

II. A Mathematical Model for DC-bus Current Harmonics on a Two-Level Converter under the SPWM Operation

In the system shown in Fig. 1, the PMSG supplies electrical power to an HVDC bus through an AC-DC converter, with details shown in Fig. 2a. To develop a harmonic cancellation scheme for the HVDC bus, it is essential to derive the mathematical model of its harmonics before the capacitor. In this study, a standard two-level AC-DC converter is considered for AC-DC conversion because it is known as the most used rectifier for PMSG based power generation system. It is assumed that the common asymmetrical regular sampling PWM is implemented in the AC-DC converter, as shown in Fig. 2b. Due to the converter switching actions, DC-link current i_{dc} will be with harmonics as shown in Fig. 2c with its spectrum. It can be noticed that significant components of the current harmonics are observed in f_c±3f_0 and 2f_c. Here, f_c is the switching frequency, f_0 is the fundamental frequency from PMSG. Harmonics in higher frequencies are not considered because of their lower impact on the DC-bus.

In our recent publication [16], the 2f_c harmonic component has been studied in detail. In this section, we will focus on the development of the mathematical models of (f_c±3f_0) harmonics.

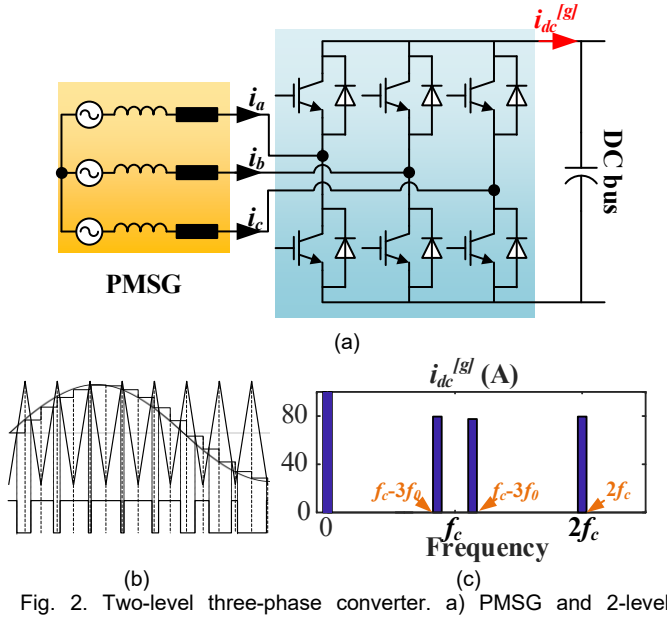


Fig. 2. Two-level three-phase converter. a) PMSG and 2-level converter, b) asymmetric regular sampling PWM, c) spectrum of i_{dc}.

A. Mathematical analysis of DC-bus harmonic based on Double-Fourier method

The double Fourier method is commonly used to study the harmonics of PWM operation [18]. Some analysis has been investigated in [16], which will be briefly reviewed here.

Assuming the current on the AC side is ideally sinusoidal for a two-level converter, AC side currents can be written as

$$i_{ac}^{[k]}(t) = I_{ac}\cos\left(2\pi f_0 t + \beta + \frac{2k\pi}{3}\right) \tag{1}$$

where I_{ac} is the amplitude of the fundamental component of AC current, f_0 is the fundamental frequency, β is the angle between phase current and its AC side voltage, k=0, 1 and 2 represent phase A, B and C respectively.

Assuming the positive current on DC bus (i_{dc}) is from the converter to the dc-link capacitor, as shown in Fig.2a. Its switching function for each phase leg can be expressed as

$$sf^{[k]}(t) = K_{0,1}cos\left(2\pi f_0 t + \beta + \alpha + \frac{2k\pi}{3}\right) + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} K_{m,n}cos\begin{bmatrix} m\left(2\pi f_c t + \theta_c^{[k]}\right) \\ +n\left(2\pi f_0 t + \beta + \alpha + \frac{2k\pi}{3}\right)\end{bmatrix} \tag{2}$$

where f_c is the switching frequency, $\theta_c^{[k]}$ is the phase angle of the triangular carrier signal for each leg, α is the phase angle between AC fundamental current and AC-side converter voltage (i.e. power factor angle), $K_{m,n}$ is the harmonic amplitude using the Bessel function of the first kind. Based on Double Fourier analysis [18], $K_{m,n}$ can be expressed as

$$K_{m,n}=\frac{1}{q_{m,n}}J_n\left(q_{m,n}M\right)\sin\left[\left(m+n\right)\frac{\pi}{2}\right] \tag{3}$$

where

$$q_{m,n}=\left(m+n\frac{f_0}{f_c}\right)\frac{\pi}{2} \tag{4}$$

In (3), $J_n()$ is the Bessel function of the first kind. m and n are orders of switching harmonic and its sidebands respectively. For instance, when m=1 and n=3, $K_{m,n}$ means the magnitude of harmonic with a frequency of f_c+3f_0. Using (1)-(4), the DC-bus harmonic currents generated from one phase leg can be derived as

$$\begin{aligned} i_{dc}^{[k]}(t)&=i_{ac}^{[k]}(t)sf^{[k]}(t)\\ &=\frac{I_{ac}}{2}K_{0,1}\left[\cos\left(4\pi f_0t+2\beta+\alpha+\frac{4k\pi}{3}\right)+cos\alpha\right]\\ &+\frac{I_{ac}}{2}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}K_{m,n}\left\{\begin{matrix}\cos\left[2\pi\left(mf_c+\left(n+1\right)f_0\right)t+\sigma_{m,n}^{[k]}\right]\\ +\cos\left[2\pi\left(mf_c+\left(n-1\right)f_0\right)t+\varphi_{m,n}^{[k]}\right]\end{matrix}\right\}\end{aligned} \tag{5}$$

where $\sigma_{m,n}^{[k]}$ and $\varphi_{m,n}^{[k]}$ are phase angles of each component, which are

$$\sigma_{m,n}^{[k]}=m\theta_c^{[k]}+\left(n+1\right)\left(\beta+\frac{2k\pi}{3}\right)+n\alpha \tag{6}$$

$$\varphi_{m,n}^{[k]}=m\theta_c^{[k]}+\left(n-1\right)\left(\beta+\frac{2k\pi}{3}\right)+n\alpha \tag{7}$$

Extracted from (5), the DC-link current harmonics in a specific frequency (if_c+jf_0) should be expressed as a sum of components from three legs as

$$\begin{aligned} i_{dc,i,j}^{[g]}(t)&=\frac{I_{ac}}{2}K_{i,j-1}\sum_{k=0}^{2}\cos\left[2\pi\left(if_c+jf_0\right)t+\sigma_{i,j-1}^{[k]}\right]\\ &+\frac{I_{ac}}{2}K_{i,j+1}\sum_{k=0}^{2}\cos\left[2\pi\left(if_c+jf_0\right)t+\varphi_{i,j+1}^{[k]}\right]\end{aligned} \tag{8}$$

where i and j mean switching and band side orders of DC-bus current harmonics. For instance, substituting i=1 and j=3 into (8) gives the expression of harmonic in the frequency of f_c+3f_0. Here we use a superscript [g] indicating this harmonic is associated with the generator connected to the AC-DC converter and is to differentiate it from the DC-DC converter harmonic which will be discussed in the later sections.

B. Harmonics on f_c±3f_0

As shown in Fig.2c, significant harmonics appear in the frequencies of both f_c-3f_0 and f_c+3f_0. Furthermore, along the whole spectrum, their magnitude cannot be ignored.

This subsection will analyse the harmonic in f_c-3f_0 firstly. Considering no phase shift on carrier signals among the three legs, i.e., $\theta_c^{[1]}=\theta_c^{[2]}=\theta_c^{[3]}=\theta_c$, substituting i=1 and j=-3 into (8) gives

$$\begin{aligned} i_{dc,1,-3}^{[g]}(t)&=\frac{3I_{ac}}{2}K_{1,-4}cos\left[2\pi\left(f_c-3f_0\right)t+\sigma_{1,-4}\right]\\ &+\frac{3I_{ac}}{2}K_{1,-2}cos\left[2\pi\left(f_c-3f_0\right)t+\varphi_{1,-2}\right]\end{aligned} \tag{9}$$

For the coefficient $K_{1,-4}$ and $K_{1,-2}$, we have

$$K_{1,-4}=\frac{2}{\left(1-4\frac{f_0}{f_c}\right)\pi}J_4\left(\frac{\pi}{2}\left(1-4\frac{f_0}{f_c}\right)M\right) \tag{10}$$

$$K_{1,-2}=-\frac{2}{\left(1-2\frac{f_0}{f_c}\right)\pi}J_2\left(\frac{\pi}{2}\left(1-2\frac{f_0}{f_c}\right)M\right) \tag{11}$$

Assuming that f_c >> f_0 (in typical cases, f_c is at least 20 times the frequency of f_0), the term f_0/f_c can be neglected as it is approximately equal to 0. Then, (9) can be approximated as expressed in (12).

$$\begin{aligned} i_{dc,1,-3}^{[g]}(t)&\approx\frac{3I_{ac}}{\pi}J_4\left(\frac{\pi}{2}M\right)\cos\left[2\pi\left(f_c-3f_0\right)t+\sigma_{1,-4}\right]\\ &-\frac{3I_{ac}}{\pi}J_2\left(\frac{\pi}{2}M\right)cos\left[2\pi\left(f_c-3f_0\right)t+\varphi_{1,-2}\right]\end{aligned} \tag{12}$$

Comparing the two terms in (12), their magnitudes have different Bessel functions and are given in (13).

$$\frac{3I_{ac}}{\pi}J_4\left(\frac{\pi}{2}M\right)\text{ and }-\frac{3I_{ac}}{\pi}J_2\left(\frac{\pi}{2}M\right) \tag{13}$$

In (13), modulation index (M) is always less than 1, because of the limited output voltage of the AC-DC converter. Comparison between the two Bessel function terms when M<1 is shown in Fig. 3. It can be seen that $J_4(\pi M/2)$ is almost zero, and $J_2(\pi M/2)$ is more than 20 times the magnitude of $J_4(\pi M/2)$.

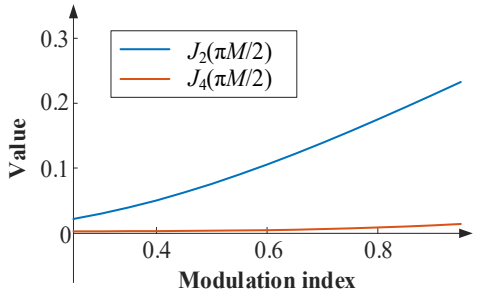


Fig. 3. Comparison between J_2(πM/2) and J_4(πM/2) with increased modulation index.

Hence, the first term is neglectable in (12). Therefore, the expression in (12) becomes as in (14).

$$i_{dc,1,-3}^{[g]}(t)\approx\frac{3I_{ac}}{\pi}J_2\left(\frac{\pi}{2}M\right)\cos\left[2\pi\left(f_c-3f_0\right)t+\varphi_{1,-2}+\pi\right] \tag{14}$$

With (14), its magnitude is convenient for a controller to calculate. There, M will be a fixed value if PMSG works under flux-weakening operation (which is a normal case for aerospace application). I_{ac} is measured by current sensors which is given as

$$I_{ac}=\sqrt{i_d^2+i_q^2} \tag{15}$$

where i_d and i_q are the d- and q-axis currents of the PMSG. Apart from magnitude, the phase angle of the component in (14) can be derived from (7) which gives the expression as

$$\varphi_{1,-2}+\pi=\theta_c-2(\alpha+\beta)-\beta+\pi \tag{16}$$

where β is the angle between phase current and its AC side voltage, α is the power factor angle. Both of them can be achieved from voltages and currents in dq-frame which are

$$\alpha+\beta=\text{atan2}(v_q,v_d) \tag{17}$$

$$\beta=\text{atan2}(i_q,i_d) \tag{18}$$

Here, the function atan2(y, x) gives the angle of complex value (x+iy). Therefore, the magnitude ($I_{dc,1,-3}^{[g]}$) and phase angle ($\theta_{dc,1,-3}^{[g]}$) of the harmonic in f_c-3f_0 can be summarized from (14) to (18) as

$$I_{dc,1,-3}^{[g]}\approx\frac{3\sqrt{i_d^2+i_q^2}}{\pi}J_2\left(\frac{\pi}{2}M\right) \tag{19}$$

$$\theta_{dc,1,-3}^{[g]}\approx\theta_c-2\text{atan2}(v_q,v_d)-\text{atan2}(i_q,i_d)+\pi \tag{20}$$

Following the same process, the magnitude and phase angle of the harmonic in f_c+3f_0 can be calculated and simplified as

$$I_{dc,1,3}^{[g]}\approx\frac{3\sqrt{i_d^2+i_q^2}}{\pi}J_2\left(\frac{\pi}{2}M\right) \tag{21}$$

$$\theta_{dc,1,3}^{[g]}\approx\theta_c+2\text{atan2}(v_q,v_d)+\text{atan2}(i_q,i_d)+\pi \tag{22}$$

From (19) and (21), it is important to notice that the simplified magnitudes of these two components of frequencies f_c-3f_0 and f_c+3f_0 are essentially the same. A comparison between the simplified magnitudes and original models is given in Fig. 4a. The error is always less than 3A, which is less than 10% of the original model. Meanwhile, the phase angle between the simplified model and the original model is also neglectable (less than 0.05 rad), as shown in Fig. 4b. Therefore, the simplified model can be adopted and used for the harmonic suppression method.

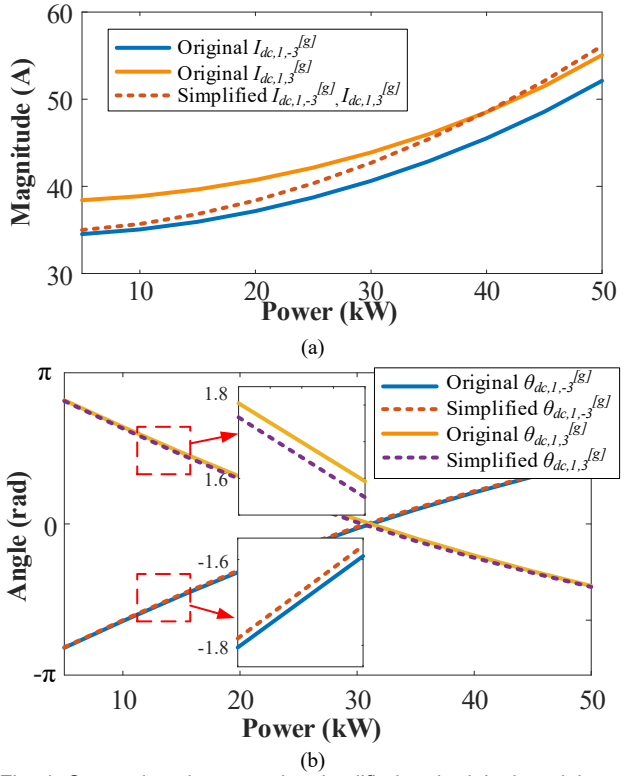


Fig. 4. Comparison between the simplified and original models on f_c-3f_0 and f_c+3f_0. a) Magnitudes. b) Phase angles.

From Fig. 4, it is important to note that the simplified magnitudes of the f_c-3f_0 and the f_c+3f_0 components will have the same increment when more power is generated from the PMSG. This is a useful finding for harmonic suppression and will be discussed in Section IV.

III. Harmonic Analysis of a DC-DC Converter

This section will discuss harmonic generated from a typical buck-boost DC-DC converter. As shown in Fig. 5, the bidirectional buck-boost DC-DC converter consists of two power switches (S1 and S2) with anti-parallel diodes and a filtering inductor L_b. The port on the left is connected to a battery with a voltage V_b, and the port on the right is connected to a DC-bus with voltage V_{dc}. This DC-DC converter allows the battery to work under both charging and discharging modes.

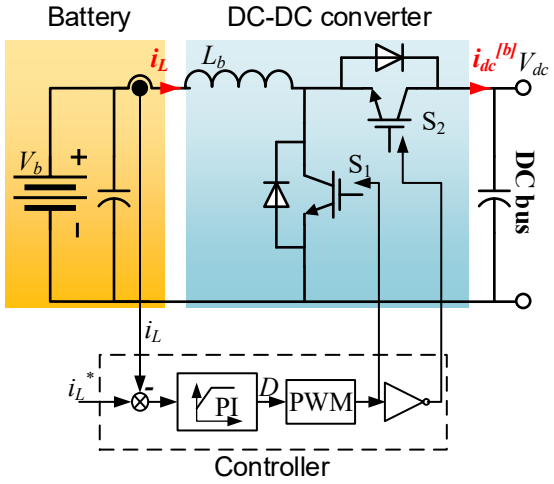


Fig. 5. Bidirectional buck-boost converter.

Within the hybrid electric power generation centre, a secondary level supervision unit is used to provide the reference power (thus defines inductor current i_L) to the DC-DC converter local control. When i_L>0, the current flow from the battery to the DC-link. The DC-DC converter operates under boost mode and the battery is in the discharging mode. On the contrary, when i_L<0, the DC-DC converter operates under buck mode and the battery is in discharging mode.

Typical PWM generation diagrams of the DC-DC converter are shown in Fig. 6a and b (battery is in discharging and charging mode). PWM signals are generated to control switches S1 and S2. The switching behaviour of these switches causes the DC-link current ripples. In Fig. 6, the switching signals are generated by comparing the duty cycle reference and carrier signal with a triangle waveform. The period of a carrier signal is defined as $T^{[b]}$. The average of the DC current $i_{dc}^{[b]}$ and its contained harmonics are dependent on the power reference (and thus i_L). Similar to AC-DC converters, the $i_{dc}^{[b]}$ harmonics phase angle can be controlled by shifting the phase angle of the carrier signal.

Similar to AC-DC converters, harmonics in switching frequencies are difficult to measure. Hence, their mathematical modelling is critical for harmonic suppression of the DC-link capacitor.

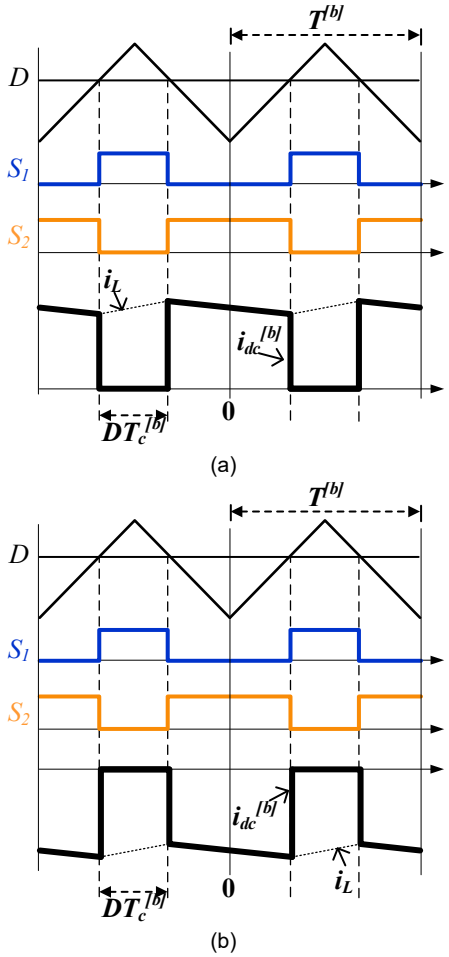


Fig. 6. Conventional PWM strategy of the DC-DC converter. a) Boost (discharging) mode. b) Buck (charging) mode.

To simplify the analysis, the inductor current is assumed to be constant as I_L, and the converter works under continuous current mode. Then, the current in one cycle flowing into the dc-bus capacitor, $i_{dc}^{[b]}$, is given as

$$i_{dc}^{[b]}=\begin{cases} I_L, & 0<t<\dfrac{(1-D)T^{[b]}}{2} \\ 0, & \dfrac{(1-D)T^{[b]}}{2}<t<\dfrac{(1+D)T^{[b]}}{2} \\ I_L & \dfrac{(1+D)T^{[b]}}{2}<t<T^{[b]} \end{cases} \tag{23}$$

Considering the symmetry and using Fourier expansion, the current $i_{dc}^{[b]}$ can be expressed as

$$i_{dc}^{[b]}=I_0^{[b]}+\sum_{k=1}^{\infty}I_k^{[b]}\cos\left(2k\pi f_c^{[b]}t+k\theta_c^{[b]}\right) \tag{24}$$

where

$$f_c^{[b]}=\frac{1}{T^{[b]}} \tag{25}$$

From (24), it can be seen that the phase angle of current $i_{dc}^{[b]}$ harmonics are related to the carrier signal phase angle $\theta_c^{[b]}$. The Fourier coefficients in (24) are derived as

$$I_0^{[b]}=I_L(1-D) \tag{26}$$

$$\begin{aligned} I_{k(k\neq 0)}^{[b]} &= 2f_c^{[b]}\int_{-\frac{1}{2f_c^{[b]}}}^{\frac{1}{2f_c^{[b]}}} i_{dc}^{[b]}(t)\cos\left(2k\pi f_c^{[b]}t\right)dt \\ &= \frac{2I_L}{k\pi}\sin(k\pi D) \end{aligned} \tag{27}$$

This paper focuses on suppressing the first-order harmonic on DC-link capacitors. Substitute k=1 into (24) and (27), the harmonic in $f_c^{[b]}$, which is $i_{dc,1}^{[b]}$ can be expressed as

$$i_{dc,1}^{[b]}=I_{dc,1}^{[b]}\cos\left(2\pi f_c^{[b]}t+\theta_c^{[b]}\right) \tag{28}$$

where

$$I_{dc,1}^{[b]}=\frac{2I_L}{\pi}\sin(\pi D) \tag{29}$$

From (29), it can be observed that the magnitudes of harmonic components $I_{dc,1}^{[b]}$ is proportional to the inductor current I_L. There, when I_L>0, the battery operates under the discharging mode. When I_L<0, the battery operates under the charging mode. With a higher output/input power, $I_{dc,1}^{[b]}$ will be with a higher absolute value. From (28), it can be seen that the phase angle of this harmonic is related to the carrier signal phase angle $\theta_c^{[b]}$. By adjusting I_L and $\theta_c^{[b]}$, active controls of magnitude and phase angle of current $i_{dc}^{[b]}$ can be achieved. The harmonic frequency $f_c^{[b]}$ can further be set to be the same as that of the targeted harmonic component on the HVDC bus. Thus, the DC-DC converter can potentially be used to cancel some specific harmonics on the DC bus as discussed in the following section.

IV. Capacitor Harmonic Minimization Method

A. Proposed method

The hybrid generation centre with more details is shown in Fig. 7. Within such a system, a PMSG supplies power to an HVDC bus through an AC-DC converter. A high-voltage battery supplies power to the HVDC bus (270V) via a DC-DC converter. Both converters share the DC-link capacitor. The AC-DC converter and the DC-DC converter are controlled with their local primary controller.

A system controller is used for high-level supervision (secondary) control. The system-level control is to define power sharing between PMSG and the battery by defining their power references ($i_{dc}^{[g]*}$ and i_L^*). The local controllers thus control converters of the PMSG and the battery individually. This way the voltage regulation can be achieved.

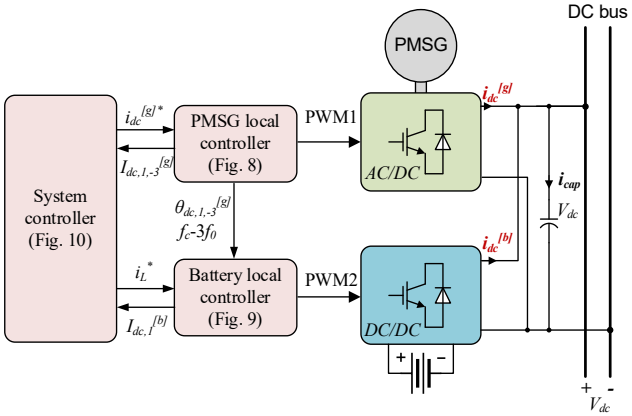


Fig. 7. Control architecture of the hybrid generation system.

This paper focuses on harmonic suppression in the frequency of f_c-$3f_0$. In Fig. 7, two converters will inject required DC currents on this frequency to the HVDC bus.

The local control diagram of PMSG is shown in Fig. 8. A cascaded control structure has been used, with the current control being the inner loop. A flux-weakening control is applied in the outer control loop. This is due to the fact that in MEA applications, PMSG is driven by the high-speed shaft of an aircraft engine. The stator output voltage $\sqrt{v_d^2+v_q^2}$ is controlled by injecting a negative flux current component i_d. The output current i_{dc} of the AC-DC converter is also controlled with its reference $i_{dc}^{[g]*}$ given by the system-level controller. With measured currents i_d, i_q, voltage references v_d and v_q modulation index M, the information of harmonic component f_c-$3f_0$ can be derived, with its magnitude $I_{dc1,-3}^{[g]}$ and its phase angle $\theta_{dc1,-3}^{[g]}$ from (19) and (20). The fundamental frequency (f_0) can be obtained from a machine speed sensor. These features of the f_c-$3f_0$ component, i.e., magnitude, frequency, and phase angle are then sent to the controller of the DC-DC converter and the system controller.

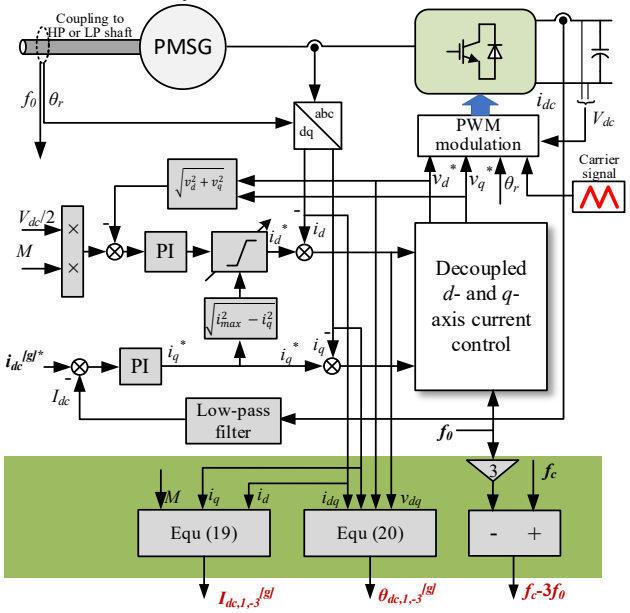


Fig. 8. Control diagram of the PMSG system.

The cancellation scheme of the harmonic component of f_c-$3f_0$ from the AC-DC converter is essentially based on the fact that two sinusoidal currents of the same magnitude will cancel each other if they are 180° phase shift to each other. With this fact, we can use the DC-DC converter as an active harmonic injection source to cancel the f_c-$3f_0$ harmonic component from the AC-DC converter. This approach has the advantage of not requiring extra hardware to the system since the DC-DC converter is an integral part of the HPGC. To achieve that, the frequency of the carrier signal ($f_c^{[b]}$) of the DC-DC converter should be set to f_c-$3f_0$ i.e.

$$f_c^{[b]} = f_c - 3f_0 \tag{30}$$

To achieve the phase angle difference of 180° between the two harmonics, the phase angle of the PWM carrier signal should be adjusted according to (20) and the battery's working status (discharging or charging). When the battery operates under discharging mode (I_L>0), both the f_c-$3f_0$ harmonic magnitudes of the AC-DC and DC-DC converters ($I_{dc,1,-3}^{[g]}$ and $I_{dc,1}^{[b]}$) are positive, which can be derived from (19) and (29). With (20), the phase angle of the DC-DC converter's PWM carrier signal should be set as

$$\theta_c^{[b]} = \theta_{dc,1,-3}^{[g]} - \pi = \theta_c - 2\text{atan2}\left(v_q, v_d\right) - \text{atan2}\left(i_q, i_d\right) \tag{31}$$

Then, a phase angle difference of 180° between two harmonics can be achieved. On the contrary, when the battery operates under the charging mode (I_L<0), $I_{dc,1}^{[b]}$ becomes negative, and thus the phase angle of the PWM carrier signal should be set as

$$\theta_c^{[b]} = \theta_{dc,1,-3}^{[g]} = \theta_c - 2\text{atan2}\left(v_q, v_d\right) - \text{atan2}\left(i_q, i_d\right) + \pi \tag{32}$$

where $\theta_c^{[b]}$ is the phase angle of the carrier signal of the DC-DC converter.

Therefore, the carrier signal frequency ($f_c^{[b]}$) and the phase angle ($\theta_c^{[b]}$) can be selected based on the harmonic information sent from the PMSG controller. The control diagram of the DC-DC converter is shown in Fig. 9. The magnitude of the $f_c^{[b]}$ harmonic from the DC-DC converter ($I_{dc,1}^{[b]}$) is also calculated using (29). This will be used in the system controller in the next discussion.

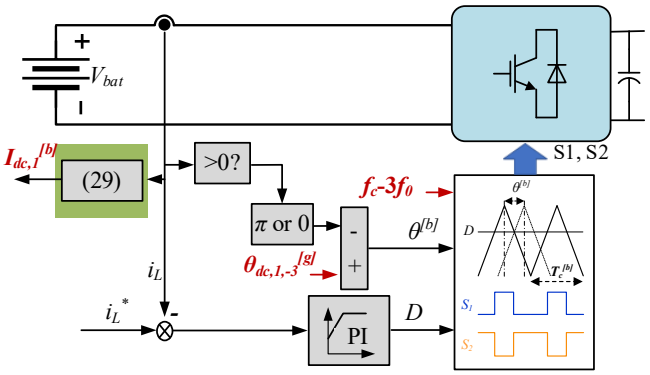


Fig. 9. Control diagram of the battery system.

The control scheme of the DC-DC controller only gives a 180° phase difference between components generated from the AC-DC and DC-DC converters. To fully suppress the harmonic on the DC-link capacitor, the magnitudes of the two components need to be adjusted to the same value. Such an adjustment is achieved in the system controller, as shown in Fig. 10.

In the harmonic control block of Fig. 10, magnitudes of two components ($I_{dc,1,3}^{[g]}$ and $|I_{dc,1}^{[b]}|$) are controlled to be the same by a PI controller. If $|I_{dc,1}^{[b]}|$ is lower than $I_{dc,1,3}^{[g]}$, the PI controller will give a higher $|i_L^*|$ to increase $|I_{dc,1}^{[b]}|$. Here, the absolute value of the magnitudes is taken to make the control feasible under either the discharging or charging mode of the battery.

Meanwhile, another PI controller gives the total DC current reference i_{dc}^* to control the DC link voltage V_{dc}. Then the reference of PMSG output current is also achieved from i_{dc}^* and i_L^* according to the discharging/charging mode of the battery.

In power management of the power generation system, the state of charge (SoC) of the battery is one of the major concerns. Generally, the SOC of a battery should be within a required range. The battery should be discharged when the SOC is over the upper limit and be charged when the SOC is under the lower limit. In Fig. 10, the system controller also integrates a SoC

controller to determine the discharging/charging mode of the battery. The drawback of this concept is that the charging and discharging speeds of the battery are limited by the harmonic suppression effect. This issue is a trade-off and can be further studied in the future.

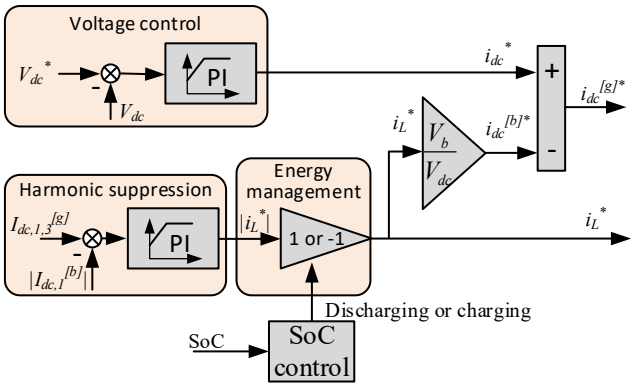


Fig. 10. System controller.

In a system without a centralized controller, the voltage control block and harmonic control block can be distributed into the local controllers of the PMSG and the battery. A similar harmonic suppression effect can be achieved. However, this is not what this paper focuses on, and will not be discussed in detail.

B. Discussion on the f_c+3f_0 harmonic component

As discussed in previous sections, the proposed method is with two actions: adjusting the switching frequency of the DC-DC converter and adjusting the power sharing ratio to control $|I_{dc,1}^{[b]}|$ to be the same as $I_{dc,1,-3}^{[g]}$. With the first action, the proposed method should eliminate the components on DC-link currents in both the frequencies of f_c and f_c-3f_0. This shows the superiority of the proposed control method when comparing to the conventional control. However, for the second action, although the magnitude of the f_c-3f_0 component is suppressed to zero, the f_c+3f_0 component (from the AC-DC converter) varies when changing the output power of the PMSG. Hence, this section will discuss the sum value of the first-band harmonics on the DC-link current.

When the f_c-3f_0 components from the AC-DC and DC-DC converters counteracted each other with a 180° phase difference, the total harmonic in the first switching band ($I_{dc,1,total}$) can be expressed using the simplified harmonic models in Section II.

$$\begin{aligned} I_{dc,1,total} &= I_{dc,1,-3}+I_{dc,1,3} \\ &= \left|I_{dc,1}^{[g]} - I_{dc,1}^{[b]}\right| + I_{dc,1}^{[g]} \end{aligned} \tag{33}$$

where $I_{dc,1}^{[g]}$ is the simplified magnitude of the f_c-3f_0 and the f_c+3f_0 components from the AC-DC converter (discussed in Section II.B), $I_{dc,1}^{[b]}$ is the magnitude of the f_c-3f_0 component from the DC-DC converter when its switching frequency is adjusted to f_c-3f_0. In (33), term $|I_{dc,1}^{[b]}$-$I_{dc,1}^{[g]}|$ is the summed absolute harmonic on the DC-link current in the frequency of f_c-3f_0 (from the AC-DC and the DC-DC converters together) and the term $I_{dc,1}^{[g]}$ is the harmonic in f_c+3f_0 (from the AC-DC converter only). Considering the value of $I_{dc,1}^{[b]}$ and $I_{dc,1}^{[g]}$, (33) can be rewritten as

$$I_{dc,1,total} = \begin{cases} I_{dc,1}^{[b]}, & I_{dc,1}^{[g]} \le I_{dc,1}^{[b]} \\ 2I_{dc,1}^{[g]} - I_{dc,1}^{[b]}, & I_{dc,1}^{[g]} > I_{dc,1}^{[b]} \end{cases} \tag{34}$$

When $I_{dc,1}^{[g]} \le I_{dc,1}^{[b]}$, and the DC-DC converter operates under the boost mode, if we increase the power of the battery and thus the power of the PMSG is decreased, then the total first band harmonics will be increased because total harmonic in this case ($I_{dc,1}^{[b]}$, as shown in (34)) will increase because of the increase of the battery power.

On contrary, when $I_{dc,1}^{[g]} > I_{dc,1}^{[b]}$, if we decrease the battery power and thus PMSG power will be increased. Then, $I_{dc,1}^{[g]}$ will increase and $I_{dc,1}^{[b]}$ will decrease. The total power ($2I_{dc,1}^{[g]}$-$I_{dc,1}^{[b]}$, as shown in (34)) will also increase because of an increased term ($2I_{dc,1}^{[g]}$) minus a reduced term ($I_{dc,1}^{[b]}$) gives a higher value.

Hence the total harmonic is at its lowest level when $I_{dc,1}^{[g]} = I_{dc,1}^{[b]}$. This proves that the proposed power sharing adjustment gives the best operation point for suppressing the total first band switching harmonics. When the battery operates under the buck mode, the harmonic is more complicated. However, with a proper phase-shift between the two converters, both the harmonics in f_c and f_c-3f_0 can be suppressed. Maybe it is not the best operation point (f_c+3f_0 could be higher), but the harmonic suppression is still effective compared to the conventional control.

V. Simulation and Experiment Study

A. Simulation study

To evaluate the performance of the proposed harmonic model and cancellation method, a simulation is implemented on MATLAB/Simulink and PLECS. It includes a PMSG, an AC-DC converter, a battery, a DC-DC converter, capacitors and the load. Some basic control parameters are given in TABLE I. In the simulation, the PMSG is the one developed in [20]. As the simulation time elapses, the simulation is divided into three cases, as shown in Table II.

TABLE I
SIMULATION PARAMETERS

Category	Parameters	Values
PMSG parameters	Rotor speed	20kRPM
	Switching frequency	32kHz
	Maximum modulation index	0.9
Battery parameters	Battery voltage	200V
	Inductance	500μH
	Switching frequency	32kHz or 29kHz
DC-link	DC-link capacitance	400μF
	Load power	40kW and 60kW

TABLE II
SIMULATION CASES

Case	Time (ms)	Output power (kW)	With/without the proposed method
1	5-10	40	Without
2	10-15	40	With
3	15-20	60	With

The simulation results are shown in Fig. 12. Before the time 10ms, the output power of the system is 40kW and no harmonic suppression algorithm is applied. The power sharing ratio between the PMSG and the battery is set as 1:1. The AC-DC converter and the DC-DC converter share the same carrier

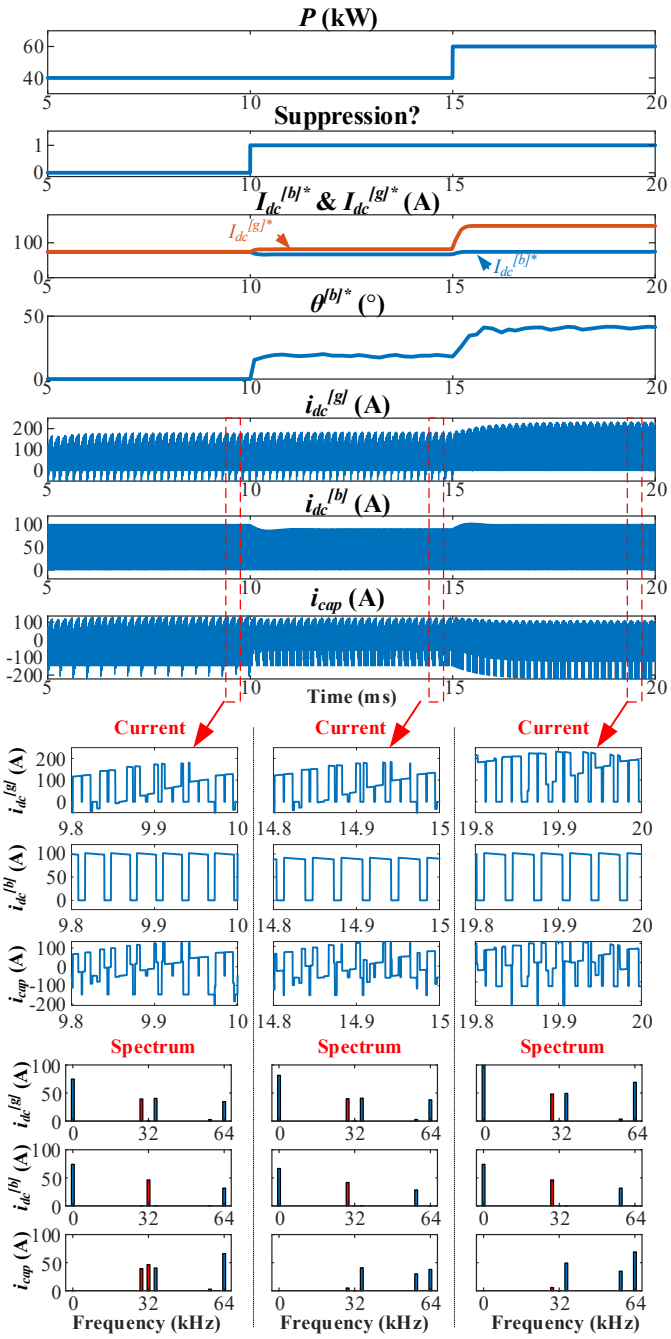


Fig. 12. Simulation results.

signal. For the DC-link currents in this case ($i_{dc}^{[g]}$, $i_{dc}^{[b]}$, i_{cap}), the PMSG generates significant components in frequencies of f_c±3f_0 and 2f_c, while the battery generates significant components in f_c and 2f_c. These components are summed up on the capacitor current (i_{cap}). Hence there are significant components shown on i_{cap} in the frequencies of f_c±3f_0 and 2f_c, as shown in the spectrum of Case 1.

Then, the proposed harmonic suppression scheme is applied at 10ms, the switching frequency of the DC-DC converter should be adjusted as f_c-3f_0 (29kHz in this case). The inductor current of the DC-DC converter is also adjusted from 100A to 90.3A to fully suppress the f_c-3f_0 harmonic on the DC-link. In the zoom-in view, the current variations are reflected on the magnitude of pulses on $i_{dc}^{[b]}$. $i_{dc}^{[g]}$ and $i_{dc}^{[b]}$ tend to counteract each other as shown in the current waveforms, and thus a suppressed f_c-3f_0 harmonic on the DC-link compared to Case 1 can be achieved, as shown in the spectrum of i_{cap} in Case 2. The f_c-3f_0 harmonic is reduced from 39.49A to 1.98A (94.8% reduction).

After the time of 15ms, the output power is required to change from 40kW to 60kW. The references of the DC-link currents change according to the new working status. With the proper power sharing and phase shift angle, a suppression of i_{cap} can be achieved when the output power is 60kW. Compared to the spectrum in case 2, the magnitudes of i_{cap} components in the frequencies of f_c+3f_0, 2f_c are increased because of higher output power of the AC-DC converter. However, the f_c-3f_0 harmonic on the DC-link is still suppressed to 2.38A. Compared to the f_c+3f_0 component (48.31A) which was not suppressed, the reduction is about 95.1%. Therefore, the simulation validates the dynamic performance of the proposed method.

B. *Experiment study*

To validate the proposed harmonic cancellation scheme, an experimental rig has been set up as shown in Fig. 11. To simplify test rig setup, PMSG is represented by a programmable AC source together with three-phase inductors. A phase-locked loop (PLL) is implemented in the controller to achieve phase angle of fundamental AC voltages. The battery is represented by a DC power supply which is connected to the DC-DC converter. Since the harmonic cancellation scheme is related to AC-DC and DC-DC converter, using a three-phase AC source and a DC power supply to represent the PMSG and battery respectively will not affect the effectiveness of the proposed harmonics cancellation scheme. The DC source is used to represent the battery with a constant voltage output of 200V. The system is controlled using TI DSP TMS320F28379D. The parameters of the experiment are shown in TABLE III. The total output power of the AC-DC converter and DC-DC converter is 2kW.The AC fundamental frequency is 50Hz. The switching frequency of the AC-DC converter, f_c, is set at 4kHz. For the proposed suppression method, the carrier signal frequency for the DC-DC converter is set to be f_c-3f_0, i.e., 3.85kHz. This frequency is a little lower than that in the case with no optimization. Therefore, this makes the following comparison reasonable.

Compared to the conventional control, the proposed method needs some extra computations, i.e., harmonic estimation from the AC-DC and DC-DC converters (in Fig. 7 and Fig. 8) and harmonic suppression control (in Fig. 10). The total

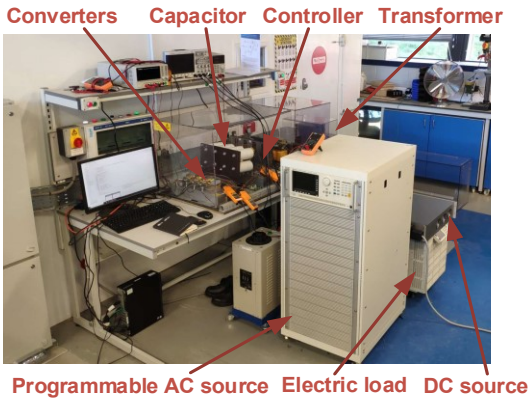


Fig. 11. Experiment setup

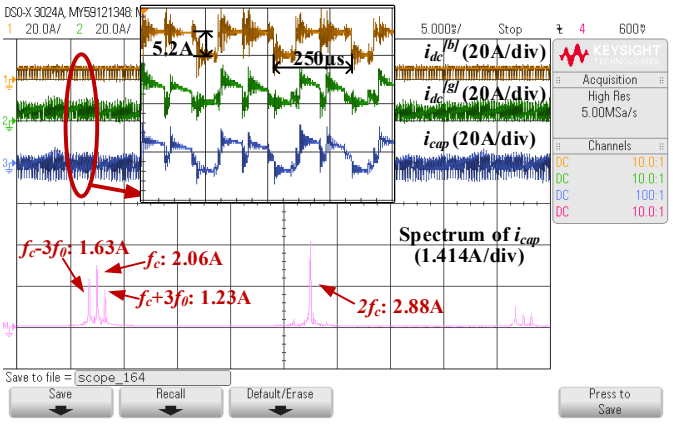
computation time of these actions is 11.7μs. In the experiment, these actions are implemented every 10ms (DC-link current control loop). Therefore, the computation intensity of the proposed method is not a problem for the system.

TABLE III
Experiment parameters

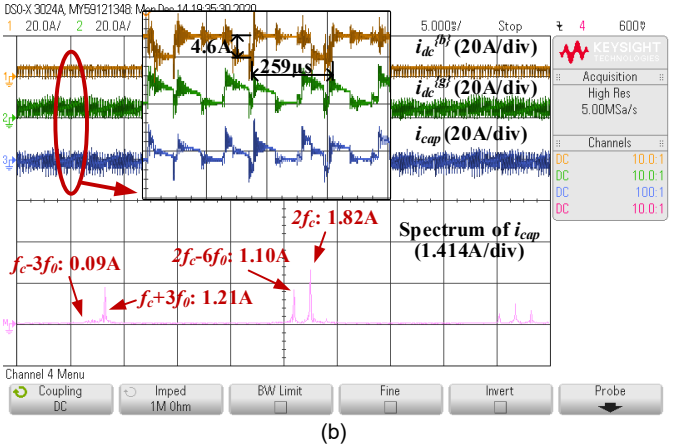
Category	Parameters	Values
DC-link	DC link capacitance	4.4 mF
	DC bus voltage	270V
	Output power	2 KW
AC-DC	Phase inductance	1 mH
	Frequencies of AC side f_0	50 Hz
	Voltages of AC side	250 V
	Switching frequency f_c	4 kHz
	Modulation index	0.90
	$i_{dc}^{[g]}$ control loop frequency	100Hz
DC-DC	Inductance	30 mH
	Carrier frequency $f_{c1}^{[b]}$	4 kHz (no optimization)
	Carrier frequency $f_c^{[b]}$	3.85 kHz (in proposed method)

Fig. 13 shows the DC-bus currents from the AC-DC converter and DC-DC converter ($i_{dc}^{[g]}$ and $i_{dc}^{[b]}$). The current flowing into the capacitor i_{cap} and its spectrum are also shown in Fig. 13. In Fig. 13a, the output power of the AC-DC and DC-DC converters are the same, i.e., $P^{[g]}$=1kW, $P^{[b]}$=1kW. Two converters use the same carrier signal. Then, results with the proposed method are shown in Fig. 13b. In Fig. 13b, the power sharing is adjusted between two converters.

With the proposed method, the switching frequency of the DC-DC converter should be adjusted as f_c-3f_0 (3.85kHz in this case). Thus, the switching cycle of the DC-DC converter is changed from 250μs to 259μs, as shown in the zoom-in views of Fig. 13a and b. From these views, the inductor current of the DC-DC converter is also adjusted from 5.2A to 4.6A to fully suppress the f_c-3f_0 harmonic on the DC-link. In zoom-in views, the current variations are reflected on the magnitude of pulses on $i_{dc}^{[b]}$. In Fig. 13b, $i_{dc}^{[g]}$ and $i_{dc}^{[b]}$ tend to counteract each other, and thus a suppressed f_c-3f_0 harmonic on i_{cap} can be achieved.



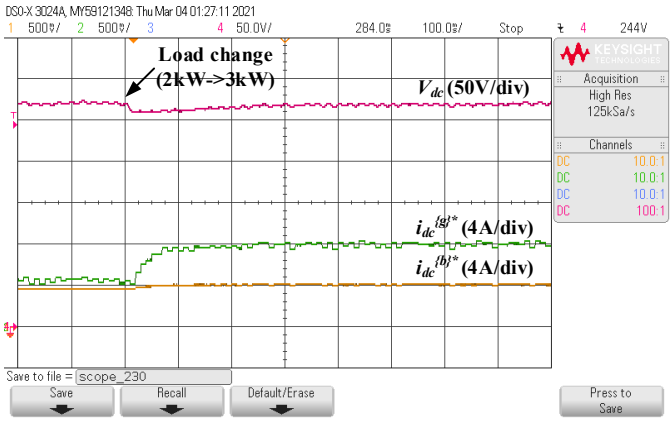
(a)



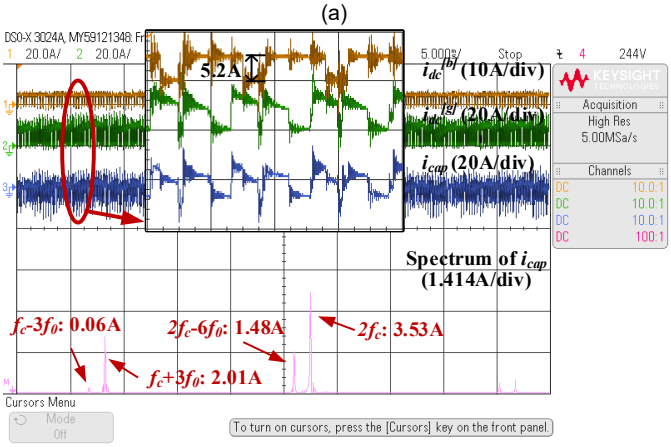
(b)

Fig. 13. Harmonic suppression when total output power is 2kW. (a) Without optimization, power sharing ratio is 1:1. (b) With the proposed method.

Comparing the two results in Fig. 13 and considering the current spectrums on the DC-link, the harmonic in f_c-3f_0 is suppressed from 1.63A to 0.09A (94.5% reduction). In f_c, there



(a)



(b)

Fig. 14. Harmonic suppression when the load power changes from 2kW to 3kW. a) Power sharing control. b) 3kW, with the proposed method.

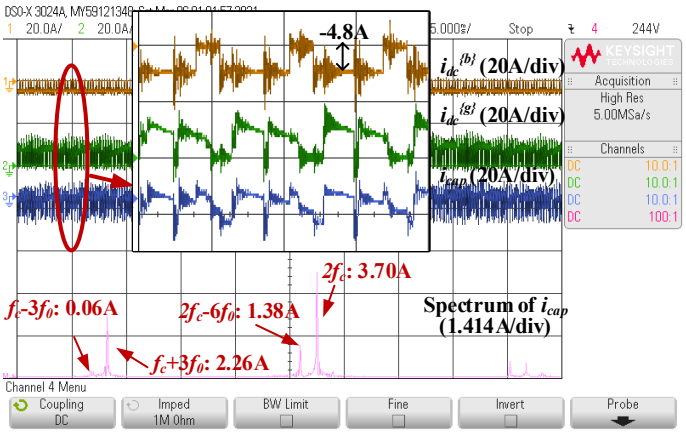


Fig. 15. Harmonic suppression when the DC-DC converter operates under buck mode, and the output power is 1kW.

is a component with 2.06A in the conventional case (Fig. 13a), but no component shown when the proposed method is applied (Fig. 13b). This is because the switching frequency of the DC-DC converter is modified from f_c to f_c-3f_0. It is also interesting to note the change of the second-order harmonics of i_{cap}. There are two components on such a band because of the change in the switching frequency of the DC-DC converter.

The DC power generation system suffers dynamic load change in the MEA. For the proposed method, the power sharing ratio should also be adjusted when such a dynamic change happens, as shown in Fig. 14a. The DC load changes from 2kW to 3kW, and it results in a DC-link voltage drop and recovery. The power sharing ratio changes according to the new working status. The DC-link current reference of the AC-DC converter ($i_{dc}^{[g]*}$) changes from 4.5A to 8.0A and the DC-link current reference of the DC-DC converter ($i_{dc}^{[b]*}$) changes from 3.4A to 3.9A. With the proper power sharing and phase shift angle, a suppression of i_{cap} can be achieved when the output power is 3kW, as shown in Fig. 14b. Comparing to Fig. 13b, the magnitudes of i_{cap} components in f_c+3f_0, 2f_c are increased because of higher output power of the AC-DC converter. However, the f_c-3f_0 harmonic on the DC-link is still suppressed to almost zero (0.06A), which validates the effectiveness of the proposed method under different output power.

Considering the SoC management of the battery, the DC-DC converter may work under buck-mode (charging mode for the battery). In this case, the proposed method can still work effectively, as shown in Fig. 15. The output power of the system is 1kW. The inductor current of the DC-DC converter is adjusted to -4.8A in this case. The pulses on $i_{dc}^{[b]*}$ becomes negative, and it counteracts with $i_{dc}^{[g]}$. Then, the f_c-3f_0 harmonic on the DC-link is suppressed to almost zero (0.06A).

VI. Conclusion

This paper proposed a DC-link harmonic suppression scheme within a DC power generation system which used a cooperation control between the AC-DC and DC-DC converters. The switching frequency of the DC-DC converter is set according to the fundamental frequency of the AC-DC converter. Then, using a simplified harmonic model and adjusting the power sharing ratio between the AC-DC and DC-DC converters, the targeted harmonic component (in our example case f_c-3f_0) has been suppressed significantly. The proposed method is feasible when the battery works under either discharging or charging modes. There is a trade-off between harmonic suppression and the charging/discharging speed of the battery. The effectiveness of the proposed method is validated by the experimental results. Furthermore, the extra computation burden of the proposed method is very low, and the DC power generation system does not need extra hardware. Thus, the proposed is convenient to implement and can preserve the simple control.

Acknowledgement

This work was supported by the Clean Sky 2 Joint Undertaking under Grant 807081. The author Cheng Wang also thanks the stipend funding from China Scholarship Council (CSC).

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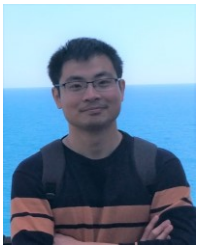

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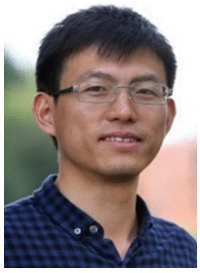

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