DESIGN AND CONSRUCTION OF A DIGITAL QUIZ-SHOW TIMER

BY

OGACHEKO SAMSON OKPANACHI
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A PROJECT REPORT SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA, NIGER STATE.

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DEDICATION

I dedicate this work to God Almighty, my parent, my uncles and all who believe in my success.
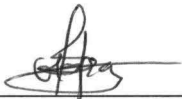
DECLEARATION

I, Ogacheko Samson Okpanachi, declare that this work was done by me and hereby relinquish the copyright to the Federal University of Technology, Minna.
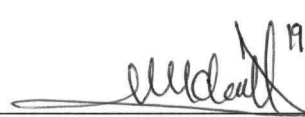
<u>OGACHEKO SAMSON OKPANACHI</u>   <u>MR. MICHAEL DAVID</u>
(Name of Student)   (Name of Supervisor)

_18/11/08_

Signature of Student   Signature of Supervisor

<u>ENGR.DR. Y. A. ADEDIRAN</u>   ---
Name of Head of Department   Name of External Examiner

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Signature of Head of Department   Signature of External Examiner

ACKNOWLEDGEMENT

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I equally use this medium to shout out to my brothers, Big bros (Emmanuel), Comrade (Amos), Tom.B (Thomas), Paulila (Paul), and to my friends, Negedu Arome Peters, you are so wonderful, I can never forget you. Afrik (Habibat), what can I say! Irawekpo, Big boy (Matthew Egene) you are the best. Important Mutum (Matthew Chukwu), God will increase you the more. Abavic (Abalaka Victor), small, but great egbe. My room mate Prof (Thomas) and D great three (Shaka, Mohammed and Haruna).O'jerry, Level (Ekele), Amana, Maduabuchi, you are all recognized. All the lecturers of the department of Electrical/ Computer Engineering, you cannot be forgotten.

ABSTRACT

The technological advancement in the 21st century made it necessary for the construction of a Digital Quiz-show timer circuit. Quiz-show timers already exist in the form of fastest first finger indicator and contest requiring a coordinator to decide who answers. The Digital Quiz-show timer in this work could be called a dual Digital Quiz-show timer where two inputs go to the circuit, one for the fastest first finger and the other for the quiz coordinator. The circuit which was built with the combination of some integrated circuits (ICs) is also intended to reset the circuit when the set time elapse.

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CHAPTER ONE

1.1 INTRODUCTION

A competition which involves testing of one's knowledge within a specified time is called A Quiz competition.

In schools, quiz competition plays an important role in influencing student performance. At the elementary, secondary, and tertiary levels, this game is increasingly becoming a form of challenges where competition(s) is/are organized amongst various schools or within a particular school or group. The contestant could be in group or individual. A quiz contest show is coordinated by a quiz master who read out the questions to the contestants, the time keeper who monitors the time and alert by ringing a bell and the recorder who is saddle with the responsibility of recording the performance of each contestant. The quiz master is also in charge of choosing any contestant who indicates by raising of hand that he/she is ready to any answer the question.

Over time there have been some difficulties faced as a result of inaccurate timing and wasting of time on reset and so on. In the clamor for fairness and efficiency. Hence the need for a digital electronic circuit is employed.

1.2 METHODOLOGY

The digital Quiz-Show Timer is design to solve the problems encountered in a Quiz game show. The circuits have been in use and it involves the use of integrated circuits (ICs).The wide range of available logic ICs has made it possible to construct complex digital systems that are smaller and more reliable than their discrete components counterparts.

Several integrated circuits fabrication technologies are producing digital ICs, the most common are the Transistor Transistor Logic (TTL), this uses the bipolar transistor as its main circuit element, the Complementary Metal-oxide Semiconductor(CMOS),uses the

enhancement-mode metal oxide semiconductor field effect transistor (MOSFET) as its principal circuit element. A family of TTL circuit is available under manufacturers numbering starting with the designation 74; these families provide various logical and functional characteristics with well specified speed, and power dissipation in its features. In the varying type of 74 series of TTL circuit, the LS series is the most popular, providing fast speed and low power dissipation [1]

In digital electronics, there are only two (2) logic states present at any point within the circuit. These voltage states are either HIGH (1) or LOW (0). the meaning of HIGH or LOW at a particular location within the circuit can signify a number of things, it may represent that one bit of a number or that an event has occurred or whether some action should be taken, this state can be a true or false statement which could be OFF or ON and in binary it is 1 or 0. It is therefore logical to use binary numbering system to keep track of information.

A binary number comprise 1 or 0 and this is the most important numbering system in digital world. In addition to the binary is the decimal, octal, and hexadecimal. They are so related that they can be converted from one numbering system to the other. The digital system mostly use the binary (1 or 0) and decimal (base 10). Though the octal (base 8) and hexadecimal (base 16), are used for large binary. Combination of the binary and binary-coded decimal (BCD), octal and hexadecimal logics is the building block for digital electronics circuit designs. It is with this knowledge and the existing circuit that give rise to this project work: Digital Quiz-Show Timer

1.3 AIMS AND OBJECTIVES

Considering the increasing Quiz-show competition on Television (TV) and various Radio stations, this project is aim at giving priority attentions to whosoever calls for it, thereby automatically disabling others from having access. It is also aim at resetting the circuit and making others have equal access to attempt the question. At this the process will be faster, the

happens as soon as the preset time elapse, by this the process will be faster. The project work is equally design to give the quiz master an opportunity of specifying who is to answer the questions, and this is made possible holding to the fact that the coordinator has the button attached to his desk.

1.4 SCOPE OF WORK

Can be used when the fastest finger contest show is to be played and when the quiz master is to decides who answers. The device is built so that it can set itself at a specified time. All this were made possible using integrated circuits (ICs) which are logic gate based.

1.5 SOURCE OF INFORMATION AND MATERIALS

The information for this project work were sourced from textbooks and journals, the internet not left out, more so not forgetting guide and advise from my supervisor. The materials used are sourced locally in Minna and some of the ICs where from Alaba market, Lagos.

1.6 PROJECT OUTLINE

This project write-up is five (5) chapters with each of the chapter having its own sub-headings.

CHAPTER ONE: This chapter contains the expository introduction, the aims and objective of the project, the methodology and source of information and materials

CHAPTER TWO: The theoretical background, brief history, previous work in this area and difficulties that limit performance.

CHAPTER THREE: This chapter comprises design and implementation of the project, also choice of components used is explained. Diagrams and illustrations well labeled and captioned.

CHAPTER FOUR: The steps taken to test the work and the measurement method are well documented. The results obtained are discussed.

CHAPTER FIVE: This chapter gives the summary of the work, the problem encountered and the recommendations.

CHAPTER TWO

2.1 LITERATURE REVIEW

Quiz-type game shows are increasingly becoming popular on television (TV) and radio stations these days, in such a game an electronic circuit are used to test contestants' reaction time. The contestant designated number is displaced with a 7-segment and a buzzer for an alert when the contestant presses his/her entry button.

The advancement in technology which brought about integrated circuit (IC) in their compact form as well as other passive and active components, such as capacitors, resistors, transistors, diode etc. It is upon this advancement that electronic circuit designers stand the challenge of designing circuit to implement the above quest.

Mr. Ane made an effort in 2003, at designing a 4-input circuit that serve as a timer and also possible to select a contestant out of four using the complementary metal oxide semiconductor (CMOS) and light emitting diode (LED) [2]. Mr. Ane circuit was used, but without an audio visual effect.

Another designer came up with his own circuit where eight (8) contestants are allowed to contest at a time. This circuit has audio alert effect and a time out indication. He used a semiconductor rectifier (SCRs). However, his display was a light effect by LEDs with different colors for each of the contestants [3]. The project is a 4-input circuit when any contestant presses the switch, the buzzer is activated, which marks the start of the time, that is one (1) sec and goes off and at the elapse of the time specified by the timer, the buzzer comes up again and as it goes off, it reset the circuit and a zero (0) will be displayed at the 7-segment showing that, any other contestant can try as long as the previous attempt was incorrect.

This project is also designed in a form where the quiz master announces who to answer and after he reads out the question, he then press the corresponding number which he

just announces and with this the quiz master determines who to answer. The timer is effective

and achievable with the use of 555 timer / oscillator.

2.2.0 THEORITICAL BACKGROUND

2.2.1 DIGITAL IC TECHNOLOGY

The ICs devices on which modern digital circuitry depend belongs to several "Logic

family". The term "Logic family" simply describes the type of semi-conductor technology

employed in the fabrication of the ICs. This technology is instrumental in determining the

characteristics of a particular device, which encompasses such important criteria as supply

voltage, power dissipation, switching speed and immunity to noise.

The most popular logic families' devices are the CMOS and the TTL. The TTL has its own

subfamilies including the popular power schottky (LS-TTL) variants[4]. The TTL was

employed in the design of this project for the following reasons;

(1) They offer a good compromise between speed of operation and power consumption.

(2) They are readily available and at low cost.

(3) They are powered by +5volt, which can easily be designed and constructed using the

regulator IC-7805.

Digital IC technology has advanced rapidly from small scale integration (SSI) with

fewer than 12 logic gates per chip; through medium scale integration(MSI) with 12 – 99

equivalent gate per chip on to large scale and very large scale integration (LSI and VLSI),

which can have ten of thousands of gates per chip, etc. ICs make our circuit smaller, the fact

being that the transistors and resistors which would be individually connected to the circuit

are all incorporated into the chip. And the cost of the ICs has greatly reduced because of the

mass production of large volume of similar devices.

The reign of ICs has made digital system more reliable by reducing the number of

external interconnections from one device to the other. Some of the limitations of the ICs

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include their inability to handle very large current or voltage, because the heat generated in such small spaces would cause temperature to rise beyond what IC can work with. The ICs cannot implement certain electrical devices such as inductor, transformers and large capacitor. The above limitation is the reason while ICs are use for low-power circuits operations, commonly known as information processing. Some other operation that require high power lever or devices that cannot be integrated are still handled by discrete components.

2.2.2 ENCODER

An encoder is intended to operate with inputs which have the feature that at any time, one input is singled out to have a logic level different from all the others. Digital systems frequently include components intended to generate signals indicating that some action needs to be taken. The priority encoder (74LS147) encodes the active-low input condition into the corresponding binary coded decimal (BCD) number output [5]. The output of this encoder is inverted by the inverter gate inside the hex inverter 74LS04, and is coupled to the BCD then to 7-segment decoder/display. The truth table is shown in table below;

Table 2.1. The truth table for the priority encoder.

A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	Q_3	Q_2	Q_1	Q_0
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Note:

H.......High voltage level (1)

L.......Low voltage level (0)

X.......Don't care

The first line in table 2.1 above shows all input in their inactive HIGH state. For this condition the outputs are all HIGH in the Binary Code Decimal (BCD) code. The second line in the table indicates that a Low at A_9 regardless of the state of the other inputs will produce an output code of 0110, which is the inverse of 1001, the BCD code for 9. the third line shows that a Low at A_8 provided that A_9 is High, will produce an output code of 0111 and the inverse is 1000, the BCD code for 8, similarly the remaining lines in the table, which equally shows that a Low at any input, provided all higher numbered input are High, will produce the inverse of the BCD code for that input [6].

2.2.3 7-SEGMENT DISPLAY

Most digital equipments have some means of displaying information in a form that can easily be understood by the user. This information is either numerical data or alphabetical. One of the simplest and most popular methods for displaying numeric digits 0 through 9 and sometime the hex character, all these can be achieved with the 7-segment display device. Although, there are contest where LED is provided for each of the contestants. By controlling the current through the LED, some segment will be light and others will not so that the desired character pattern will be generated [1].

2.2.4 OPERATING PRINCIPLE

The power supply of 220V A.C is reduced to 12V A.C by a 12V transformer. This supply is then rectified by the rectifier section, where the 12V A.C is converted to12V D.C and then to the filter, which is responsible for causing the pulsating D.C from the rectifier to a constant D.C supply and the regulator (IC_1), regulating the voltage to 5V to drive the system. The 4-inputs (contestants) are connected to the D Latch (IC_2), which was initially LOW, but becomes HIGH due to the resistors connected. When the contestants press any of the switches, the corresponding output of the latch IC_2 changes its logic state from 1 to 0. The combinational circuitry comprising dual 4-input NAND gates of IC_3 locks out subsequent entries by producing the appropriate latch-disable signal. Priority encoder, IC4 encodes the active-low input condition into the corresponding binary coded decimal (BCD) number output. The output of IC_4 after inversion by the inverter gates inside hex inverter of IC_5 are coupled to (BCD)-to-7-segment decoder/display driver IC_6. The output of IC_6 drives common-anode 7-segment display (LT543).

The audio Buzzer generator comprises clock oscillator IC_7 (555), whose output drives a loudspeaker. The oscillator frequency can be varied with the help of preset Resistor (R1). Logic 0 state at one of the outputs of IC_2 produces logic 1 input condition at pin 4 of IC_7,

thereby enabling the audio oscillator. The CD4017 IC8 is a decade counter which clock from 0 to 9. at the first clock on pin 2 the buzzer comes up and at the eighth clock at pin 9 the buzzer comes up and goes off at the ninth clock which is the last clock before the circuit is Reset. IC_7 needs +12V DC supply for sufficient Buzzer level. The remaining circuit operates on regulated +5V DC supply, which is obtained in IC_1.

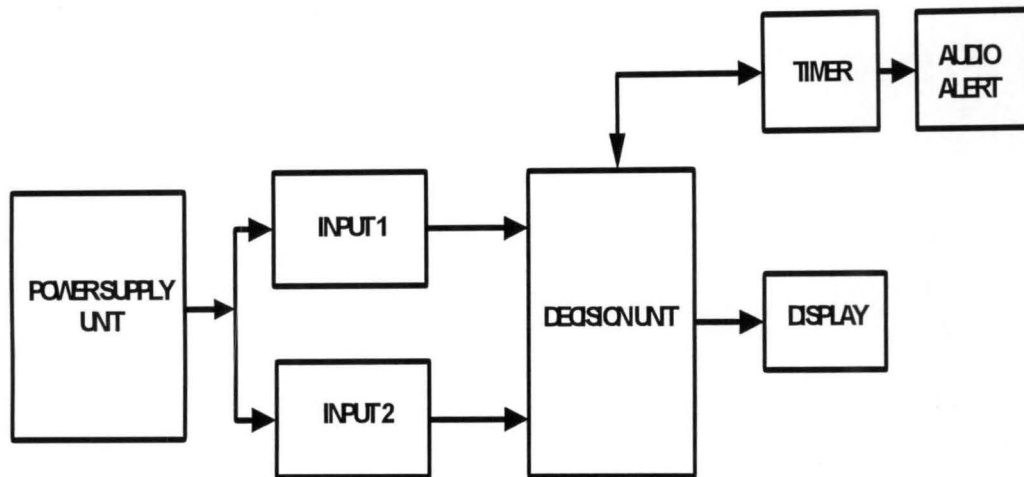# CHAPTER THREE

3.1 SYSTEM DESIGN AND ANALYSIS

Fig 3.1 Block Diagram of a Digital Quiz-show Time.

The project design Quiz-show Timer, consists of modules which were assembled to give the required design. These are; the power supply unit, the two inputs, the decision/Display unit, the timer and the audio alert.
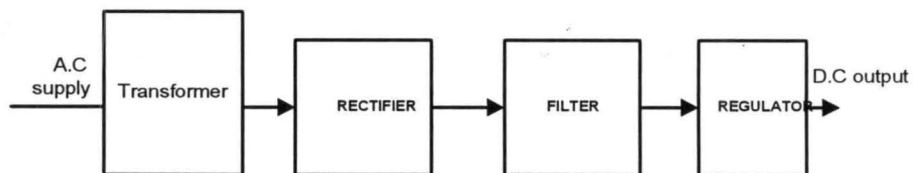
3.2 Power Supply Unit.

Fig3.2 block diagram of the power supply unit.

3.2.1 The Transformer

The first stage of the power supply design involve the stepping down of the 220v A.C from the mains to about 12V A.C with the aid of 220/12V, 500mA transformer, whose current capacity is enough to drive the entire circuit.

The transformer is an electrical device that provides electrical isolation between the 220V A.C mains and the rest of the circuit. The only link is by means of magnetic flux, thus eliminating the risk of shock. This consists of two coils, the primary (input) and the secondary (output) coil. Figure 3.2 show the circuit symbol of a transformer.

The ratio of the primary voltage V_1 to the secondary voltage V_2 is equal to the ratio of turns in primary winding n_1 to the secondary winding n_2;

220V/50Hz   12V/50Hz
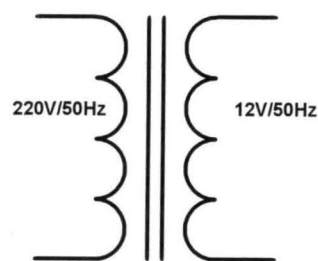
Fig 3.3 transformer windings

$$\frac{V_1}{V_2} = \frac{n_1}{n_2} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots \text{(1)}$$

A fuse (3A) is incorporated at the primary side to protect the transformer and the rest of the circuit from excessive current from the mains.

$$\frac{V_1}{V_2} = \frac{n_1}{n_2} \quad \text{...} \quad (1)$$

A fuse (3A) is incorporated at the primary side to protect the transformer and the rest of the circuit from excessive current from the mains.

3.2.2 The Rectifier

The rectifier converts the 12V A.C voltage from the transformer into a pulsating D.C voltage and this process is called Rectification.

A full –wave bridge rectifier is used for the rectification. This consist of a four (4) IN4001 diodes, with the arrangement shown below.
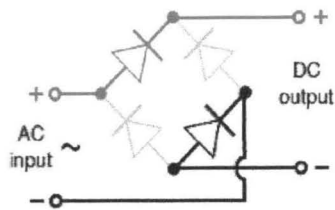
Fig3.4 Diagram of a Full-wave rectifier

During the positive half cycles, diode D2 and D3 are forward biased and current flows through any load connected at terminals AB. While in the negative half cycle, diode D1 and D4 are forward biased. Since the load current is in the same direction in both half cycles, the full-wave rectified signal appears across the load. The average D.C voltage across AB is:

$$V_{DC} = \frac{2V_{2(peak)}}{\pi} \quad \text{---} \quad (2)$$

$$= \frac{2\sqrt{2V_{(rms)}}}{\pi}$$

$$= \frac{2\sqrt{2}}{\pi} * 12 = 10.80V$$

Where $V_{2(peak)}$ and V_{rms} are the peak output and the root mean square voltages of the secondary windings of the transformer respectively.

The diode were chosen such that their peak inverse voltage (PIV) rating is greater than $V_{2(peak)}$, so that they do not break down when in reverse biased.

3.2.3 The filter

The pulsating dc voltage from the rectifier is only suitable for limited applications such as charging batteries and running dc motors. Most electronic circuits require dc voltage that is constant in value. A filter is use to convert the full-wave rectified signal into a constant dc voltage. Capacitive filtering is adopted in the design where a large electrolytic capacitor is connected across the rectifier output. The capacitor charges up during the diode conduction period to the peak value, and the rectifier voltage falls below this value, the capacitor discharges through the load, so that the load receives almost steady dc voltage. The discharge time constant, which is the time taken for the capacitor to drop to 33% of the peak value. This is given as:

$$\tau_d = R_L C \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots(3).$$

Where R_L is load resistance

And C is the capacitance.

Since R_L is a constant for any given circuit, it follows that the larger the C, the smaller the ripple voltage. A 230μf, 25V capacitor was chosen for this circuit, which is large enough for the intended purpose.

3.2.4 The Regulator (IC$_1$)

The output voltage of the filter capacitor varies when load current or input voltage varies. This effect is also undesirable. The two monolithic voltage regulator IC chips, 7809 and 7805 are used to supply steady 9V and 5V to drive the buzzer and energized the rest of the circuits respectively. These regulator chips supply the rated voltage with a wide range of

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voltage input (7V to 35V) and variation in the load current. Small capacitors (100μf) are connected at their output to filter off any ripples left on the supply line [5].
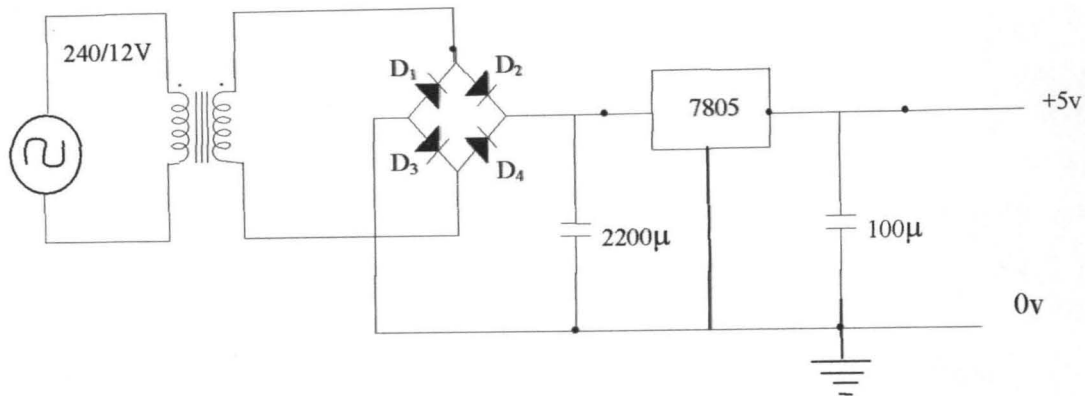
3.5 complete circuit of the power supply

The 240V AC from the mains is stepped down by the transformer to 12Vrms

Peak secondary voltage V_{sp}

$$V_{SP} = 12\sqrt{2} \quad \text{----------------------------------(4)}$$

$$V_{SP} = 12\sqrt{2} \quad = 16.9V$$

This voltage is rectified by the bridge rectifier of D1, D2, D3 and D4. The values of IN4001 were chosen since it reverse breakdown rating is many times greater than V_{sp} of 16.9 volts.

For a full wave rectifier making use of silicon diodes, the forward voltage drop for two diode $0.7 \times 2 = 1.4$ is dropped from the peak secondary voltage.

The rectified dc output $V_{dc} = V_{sp} - 1.4V_d,$ ----------------------- (5)

where V_d = Voltage drop across diode.

$V_{dc} = 16.9 - 1.4 = 15.5V$

V_{dc} is filtered to remove ripple voltages. This is achieved by the electrolytic filter capacitor C_1. The allowable ripple factor in the output voltage determines what minimal value of capacitance C_1 should have. For a pure dc supply such as a battery, the ripple factor γ is zero.

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But it is practically impossible for a rectified ac signal however; it is always desirable that the ripple factor approaches that of dc as much as possible. The ripple factor for a full wave rectified voltage is given by:

$$\gamma = \frac{I_{dc}}{4\sqrt{3}fcV_{ip}} \quad \text{-- (6)}$$

$$C = \frac{I_{dc}}{4\sqrt{3}f\gamma V_{ip}} \quad \text{-- (7)}$$

Where I_{dc} = load current

f = Frequency of the mains supply voltage

C = capacitance of filter capacitor

V_{ip} = peak full-wave rectified voltage at the filter input

The load current was calculated by summing together the system current drain as follows:

Transistor   : 3.8mA
Display   : 15.2mA
Led   : 20mA peak
_____
                39mA

Using equation (7) to calculate the capacitance

$$C = \frac{47.7 \times 10^{-3}}{4\sqrt{3} \times 50 \times 0.1 \times 15.5} = 0.000073f$$

This value of capacitance is the minimum value required to keep the 5 volt system supply regulated. A value of 2200µF capacitance was used for improved system performance.

The smoothened DC voltage was fed into a 7805 5-volt regulator to keep the terminal voltage of the DC supply constant even when the AC input voltage into the transformer fluctuates. The output from the 5-volt regulator was fed into a second 100µf capacitor C_2 which acts as a line filter to improve stability and transient response [6].

3.3 The Decision and Display Unit

This unit was designed with speed and accuracy greatly considered to achieve the desired objective.

3.3.1 Octal "D" Transparent Latch 7475 (IC$_2$)

When a contestant presses his switch the corresponding output of the latch IC$_2$ (7475) changes the logic state from HIGH to LOW

3.3.2 Dual NAND 7420 (IC$_3$)

This is a combinational circuitry comprising Dual 4-input NAND gates which is responsible to lock out subsequent entries.

3.3.3 Priority Encoder IC Chip 74147 (IC$_4$)

The 74147 IC is a high-speed SI-gate CMOS device and pin compatible with low power Schottky TTL. It is specified in compliance with JEDEC standard no. 7A. The IC is a 9-input priority encoder and accept data from nine active LOW inputs (A$_0$ to A$_8$) and provide a binary representation on the four active LOW outputs (Y$_0$ to Y$_3$). A priority encoder is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line A$_8$ having the highest priority.

The device provides the 10-line to 4-line priority encoding function by use of the implied decimal "zero". The "zero" is encoded when all nine data input are HIGH, forcing all four outputs HIGH .The priority encoder function as a decimal-to-BCD priority encoder. It is fed from the output of the Octal" Transparent Latch. This active LOW input represents the decimal digit 1 through to 9.

Table 3.1 Functional diagram of priority encoder

Pin no.	Symbol	Name and Function
8	GND	Ground (0V)
9,7, 6,14	Y_0 to Y_3	BCD address outputs (active LOW)
11,12,13,1,2,3,4,5,10	A_0 to A_8	Decimal data inputs (active LOW)
15	n. c	Not connected
16	V_{CC}	Positive supply voltage

3.3.4 Hex Inverter IC Chip 7404 (IC$_5$)

The output from the priority encoder after inversion by the inverter, 74ls04 (IC$_5$) are coupled to BCD-to-7-segment decoder/display driver.

3.3.5 BCD to 7-Segment Decoder/ Driver IC 7447 (IC$_6$)

The IC$_6$ is a low schottky BCD to 7-segment decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input-buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.[7]

The circuit accepts 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the IC$_6$ designed to withstand the relatively high voltages required for 7-segment indicators.

This output will withstand 15V with a maximum reverse current of 250µA. Indicator segments requiring up to 24mA for current may be driven directly from the IC6 high performance output transistors. Display pattern for BCD input counts above nine are unique symbols to authenticate input conditions.

The IC_6 incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time when the BI/RBO node is at HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

● Lamp intensity modulation capability (BI/RBO)

● Open collector outputs

● Lamp test provision

● Leading/trailing zero suppression

● Input clamp diodes limit high-speed termination effects

A single supply voltage is applied to this connection (V_{CC}). The LED readout may require 10 to 40mA per segment, depending on their type and size [6]

The resistor values are determined from the formula;

$$R_s = \frac{V_{CC}}{I} \text{--------------------------- (8)}$$

The current rating is assumed 15.0mA, since the rating for the IC6 is between 10mA to 40mA.

$$R_s = \frac{V_{CC}}{I} = \frac{5}{0.015} = 333.3 \ \Omega$$

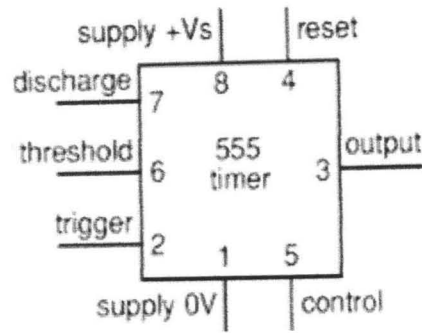Hence, 330Ω is chosen, it is readily available.

Fig 3.6 555 timer circuit symbol
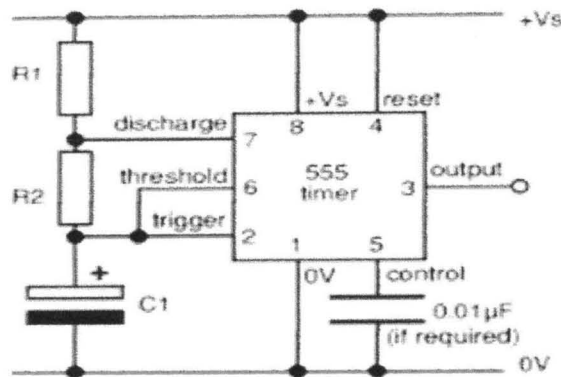
3.3.6.1 555/556 Astable

Fig 3.7 555 astable circuit

An astable circuit produces a 'square wave'; this is a digital waveform with sharp transitions between low (0V) and high (+Vs). Note that the durations of the low and high states may be different. The circuit is called an astable because it is not stable in any state: the output is continually changing between 'low' and 'high'.

Fig.3.8 555 astable output, a square wave

(Tm and Ts may be different)

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states may be different. The circuit is called an astable because it is not stable in any state: the output is continually changing between 'low' and 'high'.
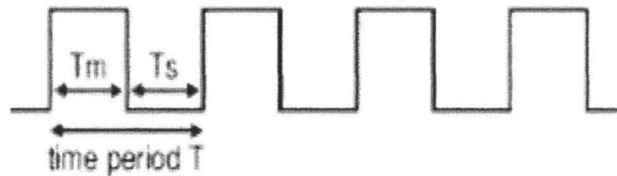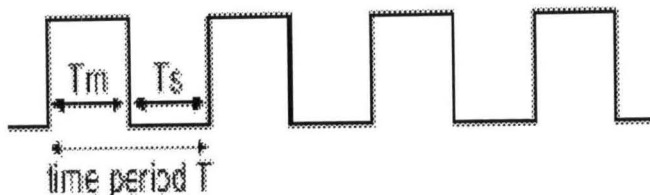

Fig.3.8 555 astable output, a square wave

(Tm and Ts may be different)

The time period can be split into two parts: **T = Tm + Ts** .... (9)

Mark time (output high): **Tm = 0.7 × (R$_1$ + R$_2$) × C$_1$** .... (10)

Space time (output low): **Ts = 0.7 × R$_2$ × C$_1$** .... (11)

Many circuits require Tm and Ts to be almost equal; this is achieved if R$_2$ is much larger than R$_1$. For a standard astable circuit Tm cannot be less than Ts, but this is not too restricting because the output can both sink and source current. The time period (T) of the square wave is the time for one complete cycle, but it is usually better to consider frequency (f) which is the number of cycles per second [9].

$$T_m = 0.7 \times (R1 + R2) \times C1 \quad \text{And} \quad T_s = 0.7 \times (R_2) \times C_1$$

$$T = T_m + T_s \qquad f = \frac{1}{T} \quad .... (12)$$

T = time period in seconds (s)

f = frequency in hertz (Hz)

R$_1$ = resistance in ohms (Ω)

R$_2$ = resistance in ohms (Ω)

C$_1$ = capacitance in farads (F)

If, R1=100k, R$_2$=100k and C$_1$=10 μf

$$T_m = 0.7(100 + 100)10^3 \times 10 \times 10^{-6} = 1.4 \text{sec.}$$

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Therefore, for the IC_8 to reset the circuit the eightieth (8th) clock which is at pin 9 was implored, because the output pulse required to reset IC_2 is taken from the pin 9

The preset time for the circuit is the T_{high} * clock number

$$T_{ime} = T_{high} \times 8 \Rightarrow 1.4 \times 8 = 11.20 \text{ sec.}$$

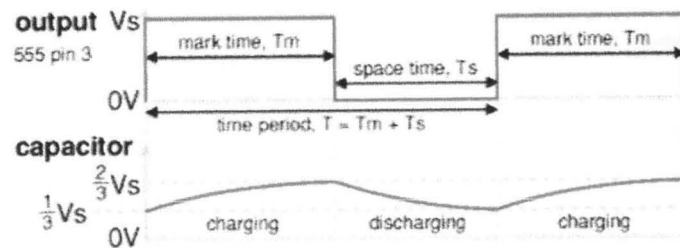Time for the project is approximately 12 seconds.

3.3.6.2 Astable operation

Fig 3.9 Waveform of Astable operation

With the output high (+Vs) the capacitor C_1 is charged by current flowing through R_1 and R_2. The threshold and trigger inputs monitor the capacitor voltage and when it reaches $^2/_3$Vs (threshold voltage) the output becomes low and the discharge pin is connected to 0V. The capacitor now discharges with current flowing through R_2 into the discharge pin. When the voltage falls to $^1/_3$Vs (trigger voltage) the output becomes high again and the discharge pin is disconnected, allowing the capacitor to start charging again. This cycle repeats continuously unless the reset input is connected to 0V which forces the output low while reset is 0V.

3.3.7 Decade counter CD4017 (IC_8)

It is responsible for the clock pulse as the IC_7 feeds it through pin 14, and shows an indication at the buzzer section. The counter hold the signal from the 555 oscillator and as it move from pin 2 to pin 11 at the clock rate according to the resistors and capacitors value of the oscillator. At the pin 11 the clock sends a signal which goes to the transistor.

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3.4 Field Effect Transistor (FET) Switch

The ease of turning ON and OFF of the switches gives it a wide application both as shunt and series switches [10].

3.5 The audio alert.

Once the contestant presses his switch the Buzzer comes on which correspond to the count of one (1) second (sec) and goes off while his number is left displaying on the 7-segment display, at the two (2) last second count the Buzzer comes up again, finally at the last second count it goes OFF and simultaneously reset the display to zero (0). The audio alert indicates an action process in electronic and are of different types having varying rating [11].

$$I_D = \frac{V_S - V_D}{R_D} \quad \text{-- (13)}$$

Where I$_D$ is audio alert current

V$_s$ is supply voltage to the transistor

V$_D$ is voltage drop across the transistor

R$_D$ is current limiting resistor

V$_D \approx 1.2$ V

$$I_D = \frac{5 - 1.2}{1000} = 3.8mA$$

Table 3.2. The truth table for the Decision unit.

A$_1$	A$_2$	A$_3$	A$_4$	A$_5$	A$_6$	A$_7$	A$_8$	A$_9$	Q$_3$	Q$_2$	Q$_1$	Q$_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
Xs	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Note:

H…….High voltage level (1)

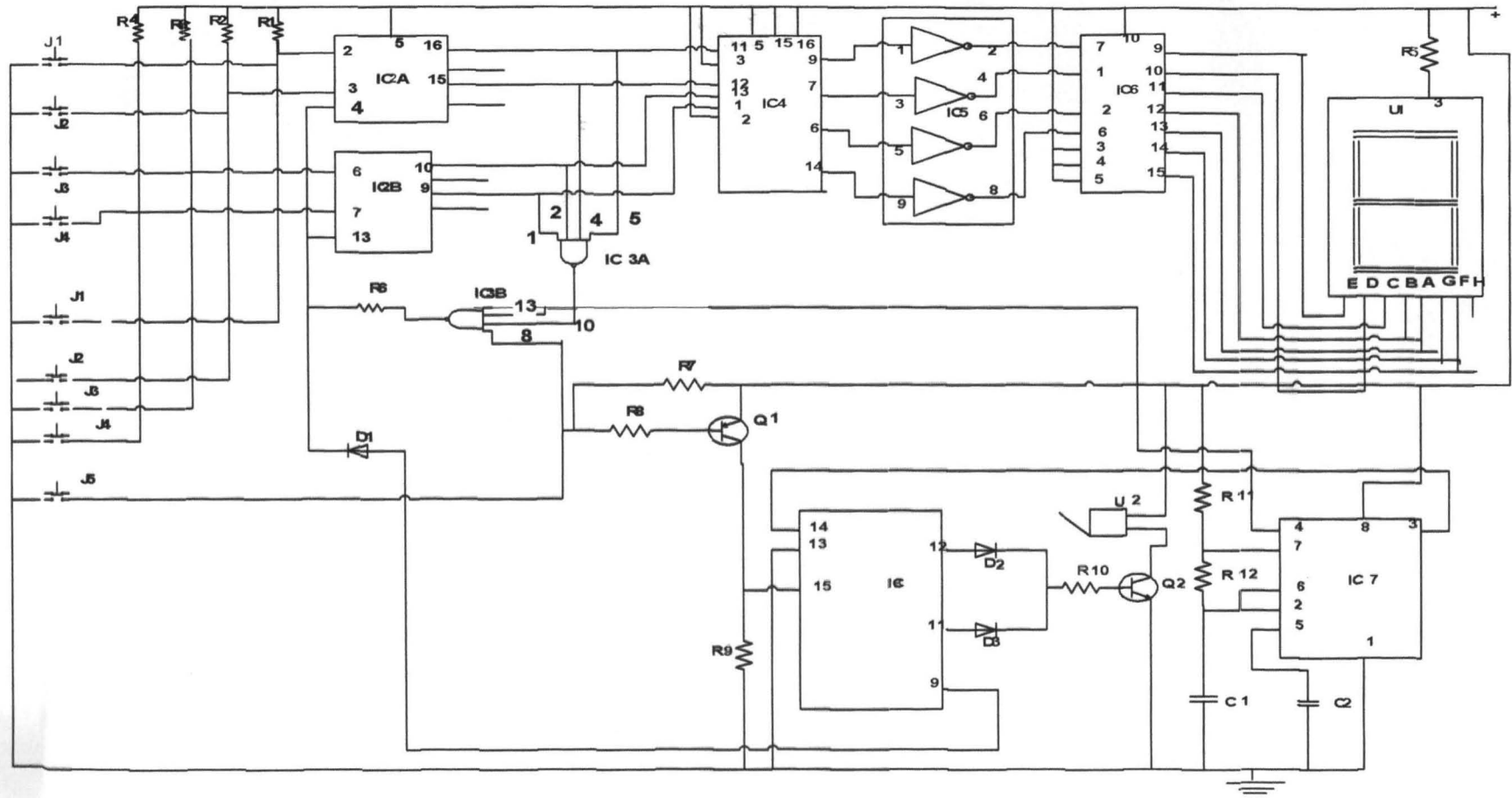L…….Low voltage level (0)

X…….Don't care

Fig 3.18 Complete circuit diagram of the Digital Quiz-Show timer

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CHAPTER FOUR

4.1 Testing/Results Obtained

At the end of the Quiz-Show Timer circuit design, the project was tested and the following were observed;

The design at the power unit was able to give the required constant 5V D.C supply for the circuit.

When the power is ON the buzzer comes up and the 7-segment display shows '0', this is so because all the inputs are HIGH.

As soon as the Quiz master presses the reset switch, the audio sound from the buzzer stops. Though the display always remain '0' at the reset either from the Quiz master or the circuit operation.

Whenever any of the four (4) contestants press the switch, the other three were disabled and they are allowed only when the circuit is reset.

The Quiz master was also a determinate to who answers, it so from the design of the project. The moment the switch was pressed the buzzer comes up and goes off. Buzzer comes up again at the eleventh seconds which indicate time up.

4.2 Discussion of Result

The project was first tested with the Quiz master deciding who to answer each question. He presses the switch at the end of the question, a buzzer comes up accompanying with the specified number displayed on the 7-segment display, then at the end of the set timing the buzzer sounded and end as the system reset itself.

The circuit was given a second test where the fastest finger on the switch was permitted to answer the question, it was equally discovered that the buzzer comes up with the number displayed on the 7-segment display; the sound also comes up at the end of the set time.

CHAPTER FIVE

5.1 Conclusion

The project work, Quiz-Show Timer was design, constructed and tested; the required working operation specified in the design was achieved. Finally, a circuit was constructed whereby the Quiz master has the option of who to answer the question at any point in time. Also the circuit can equally be used where the first contestant who is ready to answer is allowed, while other contestants are disabled, and can be given an opportunity if and only if the set time elapse and the circuit reset itself.

5.2 Recommendation

The circuit was design for four (4) contestants only, though it can be design for more contestants, this can be achieved by having more encoder connected together.

The time specified is fixed in the design; this means that the time cannot be adjusted. But the time can be adjusted by using a variable resistor.

REFERENCE

[1] Ronald.J.Tocci and Neal Widmer, "Digital systems, Principles and Application 8th

   edition prentice-hall India, 2004 pg 75-533.

[2] Gordon McComb's "Tips and techniques for the electronics hobbyist (unpublished).

[3] "Electronics hobbyist handbook", 1993 pg 33 and fig FE 34-2jpj (unpublished)

[4] B.l Theraja, A.k Theraja, "a textbook of electronics technology", 23rd Revised. Chand

   2005 pg 2555-2584.

[5] www.mitedu.freeserve.co.uk/circuits/misc/quiz.html.

[6] Musa.D.Abdullahi,"Lecture notes on Analogue Electronics January, 2005 (unpublished).

[7] Louis Nashelsky, "introduction to digital technology 3rd edition pg 171-244.

[8] Niyi Ogundana B.SC, PGD, M.SC, "Revision in electrical/Electronics Engineering

   pg121-122.

[9] www.uoguelph.ca/mantoon/circuit/555test.html.

[10] B.l Theraja, A.k Theraja, "a textbook of electronics technology", 23rd Revised.

   Chand 2002 pg 1029-1034.

[11] www.electronicsforu.com/circuitlab/electronicsbuzzer.

APPENDIX

For the Diagram in Fig.3.18

$R1 = R2 = R3 = R4 = R7 = R10 = 1K\Omega$

$R5 = 330\Omega$

$R6 = 220\Omega$

$R8 = 4.7K\Omega$

R11= R12=100KΩ

$C1 = C2 = 10\mu f$ {Electrolyte}

$D1 = D3 = N4001$

IC1=7805

IC2A=IC2B=74LS75

IC3A=IC3B=74LS20

IC4=74LS147

IC5=74LS04

IC6=74LS47

IC7=555Timer

IC8=CD4017

Q1=BC557 (NPN)

Q2=BC547 (PNP)

J1=J2=J3=J4=J5=H

U1=7-segment display

U2=Buzzer

Input 1=contestant switch

Input 2=coordinator's switch