DESIGN AND CONSTRUCTION OF A DIGITAL ELECTRONIC CLOCK

BY

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A PROJECT REPORT SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF BACHELOR OF ENGINEERING (B.ENG) DEGREE IN THE DEPARTMENT OF ELECTRICAL/COMPUTER ENGINEERING, SCHOOL OF ENGINEERING AND ENGINEERING TECHNOLOGY, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA, NIGERIA

MARCH, 2000

DECLARATION

I KAREEM KAMARU ALABA hereby declare that this project is an original concept which was totally designed, modeled and constructed by me, under the supervision and guidance of my supervisor in person of Engr. I. Danjuma

SIGNED.....

MATRIC NO.93/4103

CERTIFICATION

This is to certify that this project titled "DESIGN AND CONSTRUCTION OF A DIGITAL ELECTRONIC CLOCK" was carried out by KAREEM K. ALABA under the supervision of Engr. ISSA DANJUMA and submitted to Electrical and Computer Engineering Department, Federal University of Technology, Minna, in partial fulfillment of the requirements for the award of Bachelor of Engineering (B. ENG) degree in Electrical and Computer

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APPROVAL

This project is hereby approved in accordance with the requirements of the Electrical/Computer Engineering Department, Federal University of Technology, Minna in partial fulfilment of Bachelor of Engineering, (B. Eng.) Degree in Electrical/Computer Engineering.

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DEDICATION

This project is dedicated to my late mother, Mrs. A. M. Kareem, my father, Mr. A. Kareem, my humble brother, Mr. M. A. Kareem, my dearly friend R. A.BELO and all who have endeavoured in the infinite search for knowledge.

ACKNOWLEDGMENT

My greatest gratitude, thanks and reference goes to the most High who in His infinite mercies made it possible for me to achieve my goals academically up to this level.

My appreciation also, quickly goes to my parents, brothers and sisters whom God is using to meet my physical needs. Forever would I be grateful to them.

I would not forget my project supervisor, Engr. Danjuma, who did not let me alone during the period I needed his masterly touch on my project. He has also been a source of motivation throughout my stay in the department.

How much would I also mention of some of my friends both home and in school who were always at my reach anytime I needed their help. People like, Adewale Akinola, Rahamat, Kola, Gani, Wasiu, Mumini Fredrick, Opeyemi, Remi, Emola, Yinus, Olaleye, Popoola Bolatilo Alhaja Afusat and all those I cannot mention here due to space constraints.

I cannot fail but to acknowledgment both ASUU and NASUU of this great institution for their contribution towards our carrier and pray that may Almighty Allah sower His blessings upon everyone of them. (Amen).

I plead for the forgiveness of the those that have helped in one way or the other that have not been mentioned here and I pray that may Almighty Allah be with every one of us (Amen).

ABSTRACT

This project is about design and construction of a "Digital Electronic Clock" to indicate "Time" of the day.

The techniques employed in this project are based on a time base circuit (oscillator circuit) which generates a frequency of 1kHz. The frequency divider circuit process the signal to give an output of 1Hz. This is fed into the count accumulator of the seconds section. When the display is 59 seconds, an output is sent to the count accumulator of the minute section. Again, when the display is 59 minutes, output signal is sent to the hour section.

When the output of the hour section reads 12 hours it resets to 01 when it receive any output signal from the minute accumulator.

The logic family used in this project is the Transistor-Transistor logic (TTL). It requires a voltage between 2.4v and 5v for its operation. A regulated voltage of 5v dc supply is used to power all the Ics used in this project.

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CHAPTER ONE

INTRODUCTION

INTRODUCTION

In the world today, the increase in technological growth has made possible the construction of measuring instruments with a high degree of accuracy. As science is interested in making life more convenient for man, it is therefore necessary to ensure that little energy and time are spent on any operation. In all human endeavors especially in all laboratory work accuracy is of paramount importance. Therefore measuring instrument must possess a high degree of accuracy in which clock is an example of measuring instrument which has found it usage in the society.

Since the use of time can never be ignored it is therefore necessary to construct a device that can be used to measure time. Going down the memory lane there have being stages of development in construction of a clock. In the early days of the electronics, clock were constructed using mechanical part. They consists mainly of a gear system and a wheel balance. It was observed that after working for several hours, the teeth of the gear would wear out there by affecting the accuracy of the clock was also affected. Beside, the accuracy of the clock was also affected by the friction between the moving mechanical part and this resulted in the stiffness of the gear system .These were the problems associated, with the construction of a clock in the early days.

Nowadays, rapid growth in the electronics (digital) world makes it possible to constructed a clock with a high degree of accuracy and one that is lees tedious in its use for measurement as it is in the world to day, digital electronics is the order of the day due to many advantages associated with digital system

such as high degree of accuracy, high speed of operation and less power consumption, hence there is need for a clock to be constructed based on digital principles.

Digital system normally makes use of two possible states denoted a "HIGH" and "LOW", and "1" and a "0", "OFF" and "ON", "TRUE" and "FALSE" and hence said to operate in a binary manner. In other worlds the semiconductors are based to operate only in two logic state. By this mode of operation, problem such as thermal run away maintaing a fixed quiescent point etc common with analogue system are made void. Therefore a clock constructed based on these principles will be more accurate and efficient such a clock is said to be a DIGITAL DISPLAY CLOCK .

A digital display clock is a simple electronics device with make use of logic circuits to count and display the hours , minutes and second of the day. The clock circuit consists of time base count accumulator, decoder and display circuits.

Pulse generation is used for the time base to generated a pulse of 1 Hz (i. e one pulse per second) which is the basic count of the clock the count accumulator consists of decade counters that keep the tract of the number of seconds and minute from 00 through 59 and then resets to 00 and output of 1, pulse per minute and 1, pulse per respectively. The hour counter counts from 01, hour to 12 hours and the resets to 01 hour.(fig.1.0)

Most digital display clock finds its application and use in all aspects of life due to the fact that a high level of accuracy is guaranteed in whatever it is use for , examples of such places in which it is used are:

(a) **Electronics Systems:** It is used in electronics system such as video recorders and players to determine the time required to complete a process

, e.g in recording or determining the capacity of a recorded cassette.

(b) **Computer system**: It is use to determine the time taken to complete on operation such as formatting a disk.

(c) **Laboratories**: In a number of laboratories, digital clocks are used to find the time taken for a particular event to occur. Sometimes it is used to determine the time required to confirm the results of a particular experiment.

(d) **In sports**: It is used to determine when the time schedule for a match.

(e) **In Military Weapons** : it is use in making timing bomb and missiles

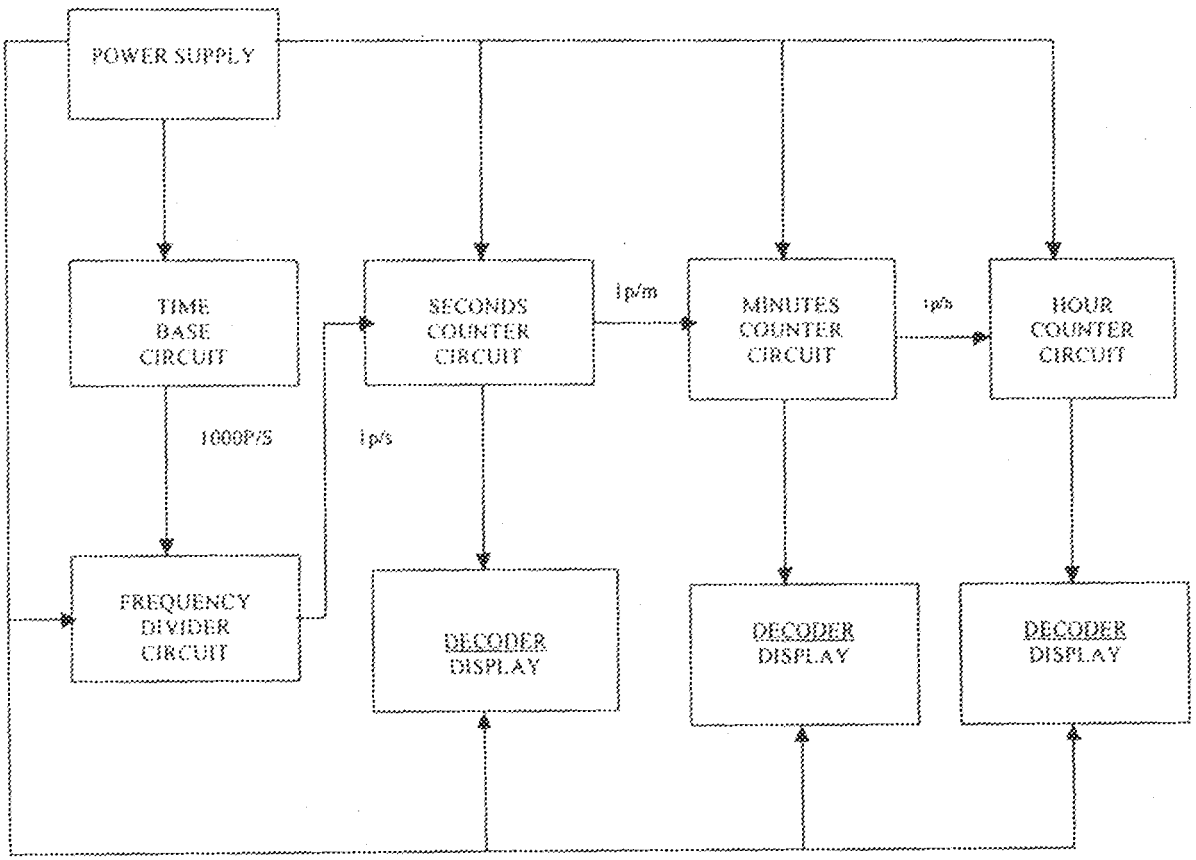


Fig. 1.0 A BLOK DIAGRAM OF DIGITAL ELECTRONIC CLOCK

1 .10 AIMS AND OBJECTIVES

The aims and objectives of this project are:

(i) To design and construct a" DIGITAL ELECTRONIC CLOCK "that will counts from 0 1 hour 12 hours and resets to 01 hour.

(ii) To design a clock of a high degree of accuracy less tedious in its use for measurement, consumption, high speed of operation and very cheap

1.2 LITERATURE REVIEW

TIME

One facet of human consciousness, is awareness of "Time " . Human being feel the passage of time in their personal experiences and also observe it in their physical environment. It has being experienced, as a one-way flow at a pace i.e show enough to be perceptible. People feel, think and act in consciousness of time flow. The irreversibility and inexorability of the passage of time is borne on every human being by the fact of "death". As the English adage says "TIME AND TIDE WAITS FOR NO MAN".

However the familiar sub-division of day into hours, hours into minute, minute in seconds taking note of the fact that, 24 hours make a day. All these facts, originates from ancient origin but has come into general usage, since 1600 AD .[1]

Moreso, going down the memory lane, there have being different types of method used in the early generation in determining time of the day in which some of them are discussed below.

1.2.1 EARLY ARTIFICIAL CLOCK

SHADOW CLOCK OR SUNDIALS

The first device for indicating "TIME" of the day is "SHADOW CLOCK SUNDIALS", when people observed that tree and other objects cast shadows which move with sun.

In 1500BC, the early Egyptians constructed shadow clock [2]. A vertical pole like

obelisk , cast, shadow on marked areas of the ground as the sun moved. The sundial works only on sunny days and when it is light but ineffective at night and on a cloudy day.

WATER CLOCKS

The problem of telling time at night or on a cloudy was solved by the ancient Egyptians with the use of "WATER CLOCK ". The water clock operate by measuring water that tricks regularly from one container to another. In 1725AD[2], the Chinese had an elaborate water-wheel clock, and later they built a 40-foot (12-metre) high pagoda-like observatory water clock.

Like the sundials , the water clock had its disadvantages i.e It would freeze in colder climates and could not easily be used no memory objects such as ships.

SAND GLASSES

Along with the development of water clocks sand glasses, which measured time by means of running from one vessels to another through a narrow passage were introduced. The sand glasses was pivoted in the centre so that it could be swelled to start the sand pouring. There exists a leather case with four sand glasses fitted so that all are visible and made to run for a quarter, half, three-quarter and one full hour.

MECHANICAL CLOCKS

The construction of mechanical clock began in the 14 the century. Although there were some primitive versions as early as 200BC [2], the first mechanical clock were sound clocks. They had no faces or hands to look at but a bell that rang a number of time each day. More advanced versions of bell clock were driven by a weight attached to a cord that was wrapped around a cylinder. The weight pull down the cord to ring the bell but such clock were not very regular or efficient.

1.2.2 PRESENT DAY CLOCK

The "PRESENT DAY CLOCKS" with hands and a dial developed and powered in different ways.

PENDULUM CLOCK

In 1656, Christian Huggen, a Dutch scientist, built the first pendulum clock [2] while in 1675, he built another clock power by a spring that regularly coiled and uncoiled.

WATCHES

In 1500 AD, Peter Helein made the first watches in Germany. They were elaborate, expensive toys of the rich that kept time quite poorly.

ATOMIC CLOCKS

The early clock were not very regular or accurate. They were affected by gravity, location, movement, wear, and temperature, and they needed constant correction. A pendulum clock would be of little use in a tossing ship at sea. The movements of such thing as a shadow , sand water, fire, sun, moon, and stars are not sufficient to measure the changes of atonic particles or the movements of bodies in outer space .

For these purposes , scientist needed a steady and detailed standards that also were being affected as little as possible by external influences. They eventually found the answer in atoms themselves. Scientists determined that, the regular predictable vibrations (also called waves, cycles, oscillations and resonations) of certain elements could function as a time standard.

The no of oscillations of element caesium in one second is 9, 192, 631, 77. In 1967, this number of oscillations has adopted in the International system of nuit (S.I) as the definition of one second. Years are now official measured in second, which at one time was based on astronomical observation, has given up, although it is still used for certain purposes. The atomic clock only in accurate by one second in many thousands

CHAPTER TWO

PROJECT DESIGN AND THEORY

INTRODUCTION/PRINCIPLE OF OPERATION

The most basic representation of an electronic clock is shown below in fig. 2.0

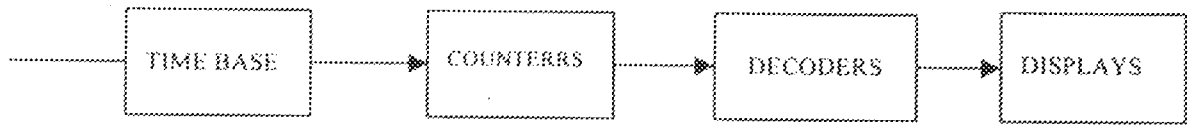


Fig. 2.0

2.1.0 SYSTEM OVERVIEW

The digital clock is a system consisting of logic gates, flip-flop and subsystems. The input of the system is the frequency source or the oscillator circuit. The processing takes place in the frequency divider, count accumulators and decoder sections. Storage takes place in the count accumulator. The control section is the time set control. The output is the digital time display. There is a power supply also to keep the system running. In fig. 2.1.0 is shown a block diagram of the digital clock. The various sections are discussed in the following sections.

BASIC OPERATION OF 555 TIMER

As shown in Fig. 2.1.1 (iii), the inverting input of the cooperator is biased at a voltage of 10v i.e [10/(5+10] 15 = 10v through a potential divider. The non-inverting input voltage of the comperator is refered to as THRESHOLD VOLTAGE and the inverting input voltage as the CONTROL VOLTAGE. When the RS flip-flip set, i.e with a voltage equal to the supply voltage at output Q and output $\bar{Q}$ at Ov, the high voltage at Q drives the transistor into saturation and this causes capacitor C which was earlier charged through resistor R to discharge through the transistor to the ground since at saturation, the transistor causes a short circuit across the capacitor. This brings the threshold voltage to OV since this is now the voltage across the capacitor C as a result of the short circuit. The comperator output is now inverted since the control input voltage is more than the threshold voltage. If a signal is applied to input R, output $\bar{Q}$ is reset to OV and output Q to 15V. Since Q output is now OV, this causes the transistor to cut-off giving way to the capacitor increase exponentially as shown in fig. 2.1.1 (iv) above and this is the same as the threshold voltage. As the capacitor charges up towards the supply voltage, immediately the voltage is slightly greater than 10V, the output of the comperator switches state leaving S input high i.e 15V. This sets the flip-flop and output Q now becomes high (15V). This process is repeated so long as the supply voltage remains. The output waveform is as shown in fig. 2.1.1 (iv).

It is important to note that the rate at which the output voltage switches state depends on the rate of charging and discharging of capacitor C. Therefore, R and C in series determine the frequency of the output waveform. The threshold voltage is exponential in nature as it is the same voltage across the capacitor.

2.1.2 REALIZATION OF FREQUENCY USED WITH 555 TIMER CONNECTED AS ASTABLE MULTI VIBRATOR. (CLOCK FREQUENCY CALCULATION)

The frequency formula for the NE555 timer is given as

$$F = \frac{1}{T} = \frac{144}{(R_1 + 2R_2)C}$$

For a frequency of 1000Hz, a capacitive value of 0.1μF is chosen

$$1000 = \frac{144}{(R_1 + R_2)(0.1X10^{-6})}$$

$$(R_1 + 2R_2) = \frac{144}{1x10^3 x0.1x10^{-6}}$$

$$= 1.44 \times 10^4$$

$R1+2R2 = 14400$

A standard resistive value of 680Ω is chosen for R1

$\therefore$ $2R2 = 14400 - R1$

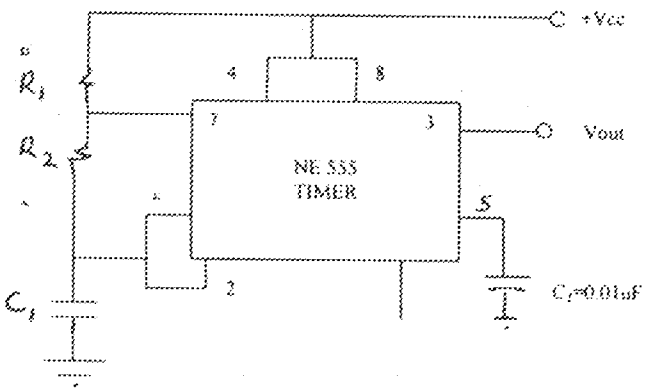
$= 14400 - 680$

$= 13720$

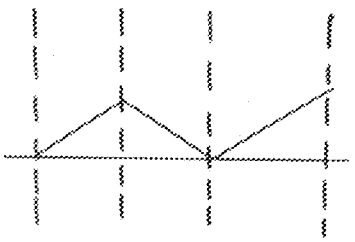
$$R2 = \frac{13720}{2}$$

$= 6860\Omega \approx \underline{6.8k\ \Omega}$

2.1.3 OPERATION OF 555 TIMER CONNECTED AS ASTABLE MULTIVIBRATOR

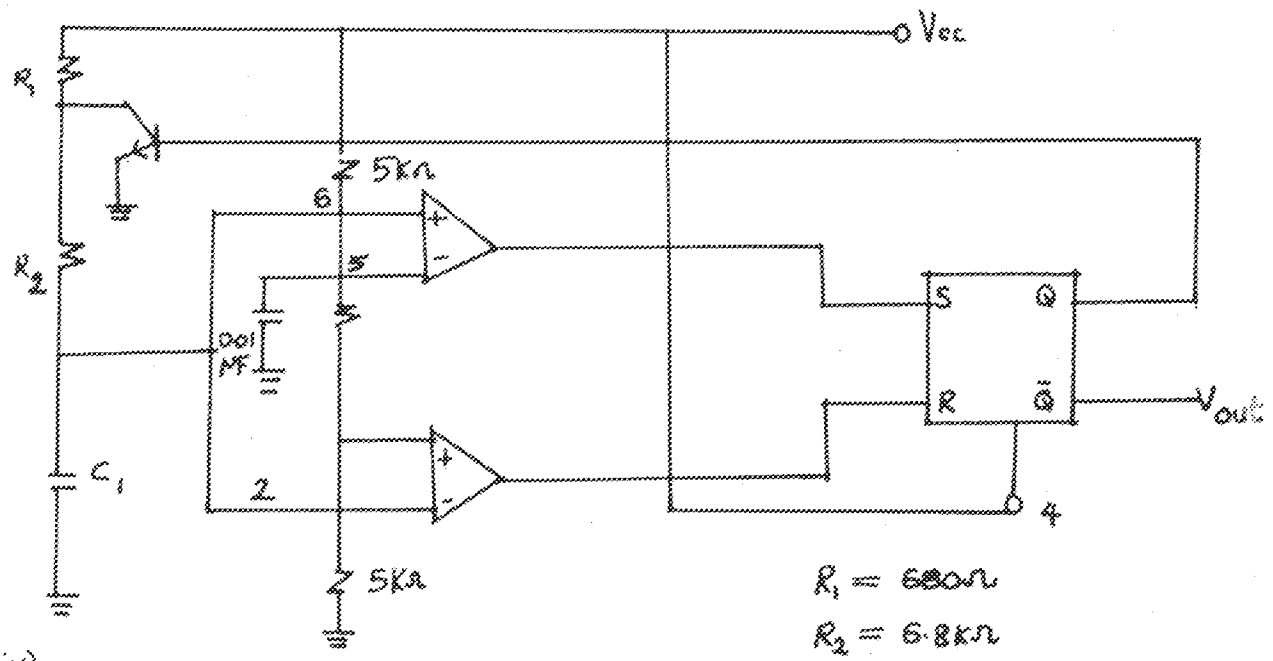


(i)



(ii) Voltage waveform of capacitor C1

(iii) Waveform of charging and discharging of capacitor C.



(iv)

fig 2.1.3

The figure shown above fig. 2.1.3 (iv) is a 555 timer connected as an astable multi vibrator (free running multi vibrator). The inverting input called the trigger (pin2) of lower comparator is connected to the threshold input (pin 6) and these two points are now connected across capacitor C. When the voltage at pin 2 is a little lower than one third of Vcc, the output of the lower comperator becomes high and this resets the flip - flop leaving Q at logic zero. This forces the discharge transistor to its cut-off region and as the collector of this transistor is connected across R2 and capacitor C at pin7, no current flows though the transistor and all the current from the supply flows through R1 and R2 to charge up capacitor C. As this capacitor charges up, the voltage across it rises first to ⅓ Vcc. When this voltage rises slightly above this value, the voltage at the inverting input of the lower compositor is greater than the voltage fixed at the non-inverting input and the output of the comparator goes low. This has no effect on Q output. The voltage across C continues to increase until it is slightly above ⅔ Vcc. Then, the threshold voltage is slightly greater than the voltage at pin 5. This turns the output of the flip-flop high and sets the flip-flop which implies that Q = Vcc. This voltage drives the discharge transistor into a saturation and then short circuits pin 7 to the ground as explained on its basic operation. The voltage at pin 7 is grounded meaning that capacitor will now discharge through R2 and via the discharge transistor to ground. The voltage across the capacitor begins to fall until it gets to ⅔ Vcc and slightly below this, the upper comparator output is switched low. But this does not affect the output Q. The voltage across C fails to ⅓ Vcc and slightly below it, the output of the lower comparator then switches high. The Rs latch is then reset and the process is repeated. The continues charging and discharging of capacitor C results in the rectangular waveformed at the output pin (3) as it is shown in fig.2.13b (iii) The wave form of the

voltage across capacitor C also decreases and increases exponentially as shown in the fig. 2.1.3. (ii). The capacitor changes up to ⅔ Vcc and discharges up to ⅓ Vcc. The by-pass capacitor (0.01μf) connected to pin 5 is just to provide noise filtering for the control voltage. If the reset terminal (pin4) is connected to the ground, it will not inactivate the whole circuit and hence it is always connected to the supply terminal as shown in the figure above.

However, having calculated the values of R1 = 6.8KΩ with chosen values of a standard resistor R1 = 680Ω and a capacitive value of 0.1μF for a frequency of 1000 Hz, this NE 555 timer is able to function as determined. Besides, in order to generate one pulse/second (1Hz) the output of this astable multi vibrator is connected to three decade counters in cascade for frequency division.

2.2.0 FLIP-FLOPS

Sequential logic circuit are derived from various inter connection of FLIP-FLOPS. They are circuit with the ability to retain present state at the output when the input states are charged. Such circuits are COUNTERS, REGISTERS, PULSE GENERATOR etc.

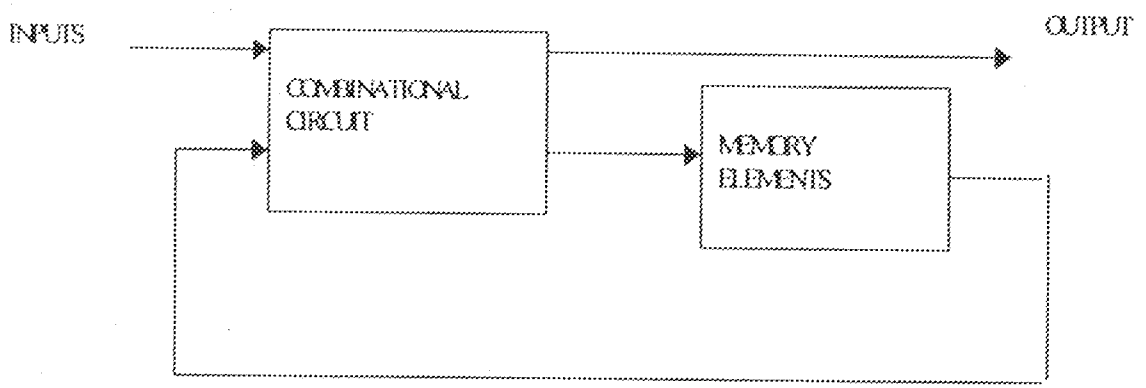


Fig. 2.2.0

The are two types of sequential circuit and they are:

(i) **ASYNCHRONOUS SEQUENTIAL LOGIC CIRCUIT SYSTEM:** Is a system which depends upon the other in which its input signals charge and can be affected at any instance of time.

(ii) **SYNCHRONOUS SEQUENTIAL LOGIC CIRCUIT SYSTEM:** Is a system which has a behaviour that can be defined from the knowledge of its signals at discrete instants of time.

The sequential logic circuits which consists of memory element are called FLIP-FLOPS. There are different kinds of flip-flops such as J.K flip-flops, D-flip-flops etc., but we will limit ourselves to the types used in this project (J-K flip-flops).

Flip-flops have the following basic characteristics.

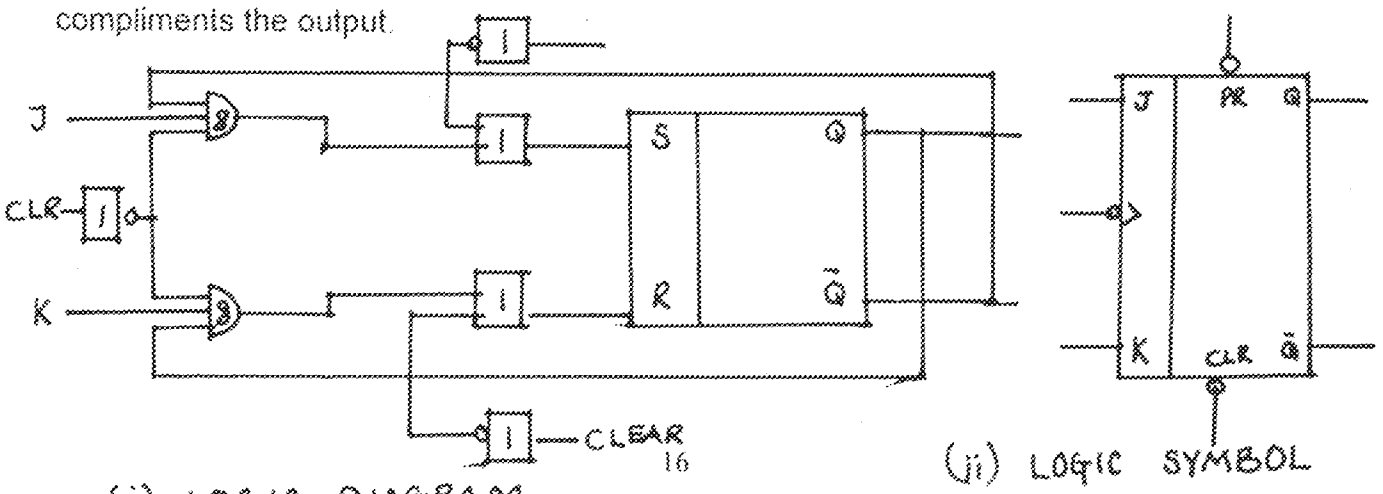
(i) They have the ability to store one bit of binary information.

(ii) They have two outputs which are complementary i.e one for the normal value and the other for the complementary value of the bit stored in it.

A flip-flop circuit can maintain a binary states indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch state.

2.2.1 J-K FLIP-FLOPS

J-K flip-flops is one of the memory elements used for counters. This is a refinement of the R-S flip-flops in that the indeterminate state of the R-S flip-flop is defined in the J-K flip-flop. When this occurs, i.e J = 1 and K = 1, the circuit toggles and complimenis the output.



(i) LOGIC DIAGRAM (ii) LOGIC SYMBOL

As it can be seen from table 2.2.1(i) the two asynchronous inputs are considered with other inputs separately because they (asynchronous inputs) are not operated simultaneously. The two asynchronous inputs affect the flip-flops independent of the clock and the two synchronous inputs i.e J and K. for example, when CLR =O, irrespective of what CLK, J or K inputs, the output is maintained at Q = O. Also when PR = O, Q = 1 irrespective of CLK, J and K inputs.

STATE OR TRANSITION TABLE: This is also one of the important table of a J - K flip - flops. The time sequence of inputs, outputs and flip-flop states are being enumerated. It consist of three section Viz, the present state, the next state and the output. The state table for the J-K flip-flop is shown in the table below.

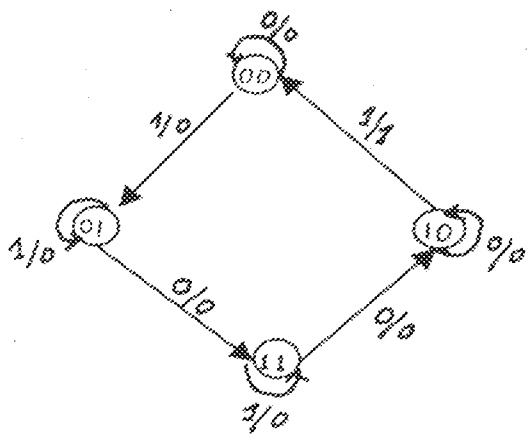
Present State of the Output	Next state of the output	Inputs	
Q	Q (t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Table 2.2.1 (ii) THE EXCITATION TABLE OF A J-K FLIP-FLOP

From the table shown above, it can be seen that when J = 0, K can either be 0 or 1 and yet, it will not affect the state of the output i.e Q = 0, Q (t+1) = 0 meaning that the J input determines the output. This is also the case when J = 1. When K = 1, J can either be 1 or O. This will make no difference at the output since K now determines the state of the output. Hence, x represents the "DON'T CARE" condition i.e it can be either 0 or 1 implies that it really makes no difference.

The present state on the table represents the state before the occurrence of the clock pulse, while the next state is the state of the output of the flip-flop after the occurrence of the clock pulse.

STATE DIAGRAM: This is a graphical representation of information on the state table. It also describing the behaviour of the logic states of a flip-flop. In this diagram, a state is represented by a circle and the transition between states is indicated by directed lines connecting the circles. An example of this is shown in fig. 2.2.1 (ii) representing the state diagram of a particular sequential logic circuit.



STATE 2.2.1 A STATE DIAGRAM OF A LOGIC COUNTER

The binary number inside each circle identifies the state it represents. The direct lines are labeled with two binary numbers separated by a slash (/). The input value causes the state transition is labeled first, the number after the symbol/gives the value of the output during the present state eg. The direct line from the state 00 to 01 is labeled 1/0 meaning that the sequential circuit is in a present state 00 when x = 0 and Y = 0 and that on the termination of the next pulse, the circuit goes to the next state, 01, and x and Y are inputs. A direct line connecting with itself indicates that no change of state occurs.

Besides, the state diagram provides the same information as the state table. There is no difference between a state table and a state diagram except in the manner of representation. The state diagram gives a pictorial views of a state transition and in a form suitable for human interpretation of the circuit operation. It is often being used as the initial design specification of a sequential circuit.

STATE EQUATION: This is also known as an application equation. It is also used to describe the behaviour of the logic state of a flip-flop. It is an algebraic expression that specifies the condition for a flip-flop state transition. The equation is obtained from the k-map. A state equation is similar in form to a flip-flop characteristics equation, accept that it specifies the next state condition in terms of external input variable and other flip-flop values. The left side of the state equation denotes the next state of a flip-flop, and the right side, a Boolean function that specifies the present state condition that makes the next state. An example of a state equation is

$$A(t+1) = (AB + AB + AB)X + ABX$$

The equation is obtained from say flip-flop A. A (t+1) represents the next state of A when the condition representing the present states of the right hand state

of the equation is met after the occurrence of the clock pulse. The time t in A (t+1) shows that it is applicable only in clock sequential circuits.

2.2.2 COUNTERS

Counter circuit is a sequential circuit which goes through a prescribed sequence of states when input pulses are applied. These input pulses are called "COUNT PULSES".

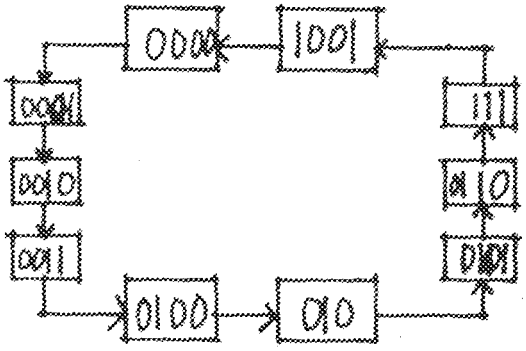
Counters generally obey the rule 2^n when n represents the number of flip-flops needed to implement a counter that will count through 2^n n number of states in binary. The largest binary number counted by n cascaded flip-flops has a decimal equivalent of 2^{n-1}. It should be noted that counters can be designed to skip some states depending on what is in the mind of the designer. Such counters are called "TRUNCATED COUNTERS".

There are two major categories of counters namely, synchronous and Asynchronous counters.

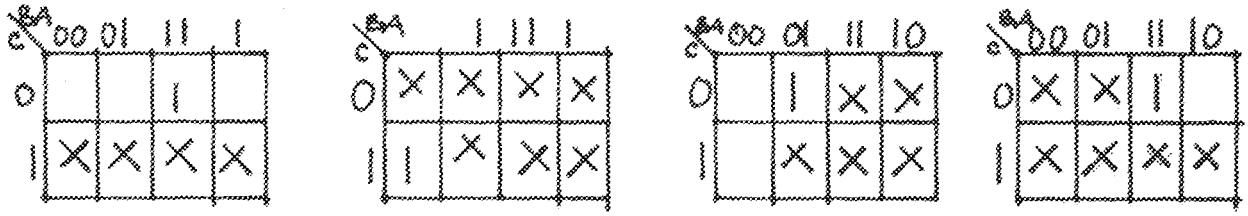
SYNCHRONOUS COUNTERS: This is the type of the counter when the flip-flops are connected in such a way that they are triggered almost at the same time by the same clock pulse (parallel connection).

ASYNCHRONOUS COUNTERS: These are obtained from serial connection of flip-flops. The disadvantage of this connection is the speed which is low since the output of one flip-flop is used to trigger the other and so on, which results in a cumulative setting time.

With all the necessary information on J - K flip-flops in the previous section, therefore we proceed to design counter (mod-10 counter) Decade counter used for this project.

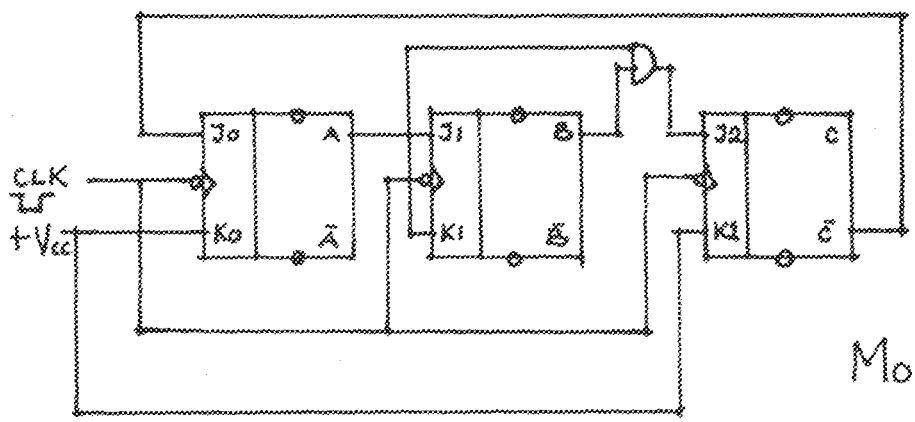


State diagrams (Mod-10 counter)

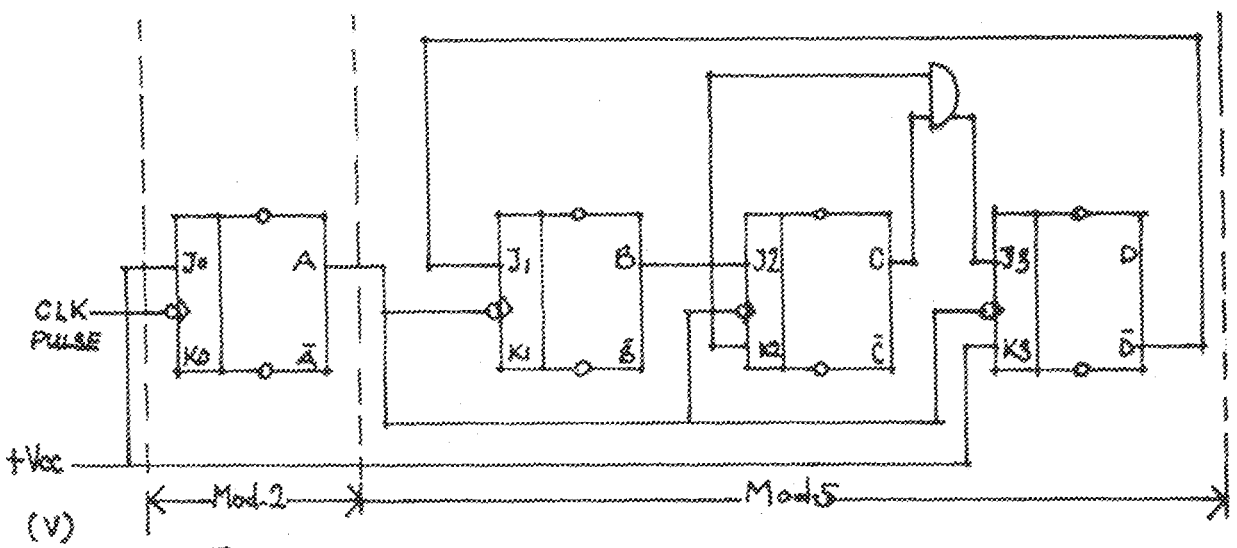


(iii)

K-maps to implement the state table



(iv) Mod-5 counter



(v)

Fig 2.2.3 Mod-10 Counter

2.3 FREQUENCY DIVIDER SECTION

The purpose of the frequency divider section is to divide the output frequency of the 555 timer (1000Hz) down to one pulse per seconds or 1Hz which is the basic count of the clock. The counters used for this purpose decade counters (74 LS 90)

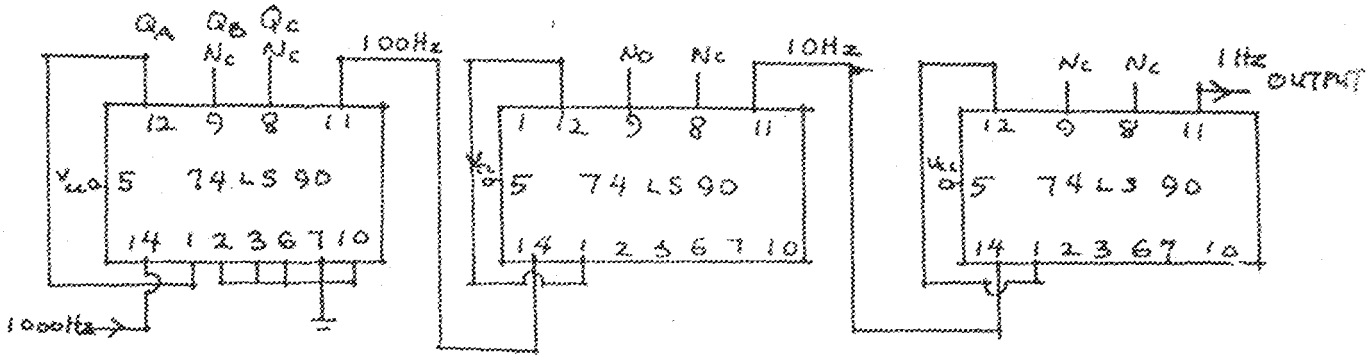


Fig. 2.3 Frequency divider circuit

2.4 THE COUNT ACCUMULATOR SECTION

This consists of counters (74 LS 90) that keep track of the number of seconds from 00 through 59 and then resets to 00 with an output of one pulse per minute. The minutes counter receives the one pulse per minute output pulse from the seconds counter as its own input and then counts the number of minutes from 00 to 59 and then resets to 00. The output of this circuit is one pulse per hours. The one pulse per hours counter counts from 01 hours to 12 hours and then resets to 01 hours.

The counters used in the seconds and minutes count accumulators (0-59 counter) consists of a decade counter. Cascaded with a 0-5 counter (i.e module - 6 counter). The decade counters are coupled with 1's place of the display. The modulo - 6 counter is coupled with the 10's place of the displace. In like manner,

the hours count accumulator is a decade counter cascaded with a 0-1 counter which is a flip in this case. The decade counter is coupled to the 1's place of the display while the flip-flop is connected to the 10's place of the display.

2.4.1 SECONDS AND MINUTES COUNTER

The seconds counter is two 7490 IC counters. The first is wired for a decade count to provide the units seconds. These two counters effectively carry out a count of 0-59 and then resets. The output is one pulse per minute which is applied to the minute counter. The minutes counters are exactly the same with an output of one pulse per hour. The seconds and minutes counter, circuit is shown below in fig. 2.4.1.

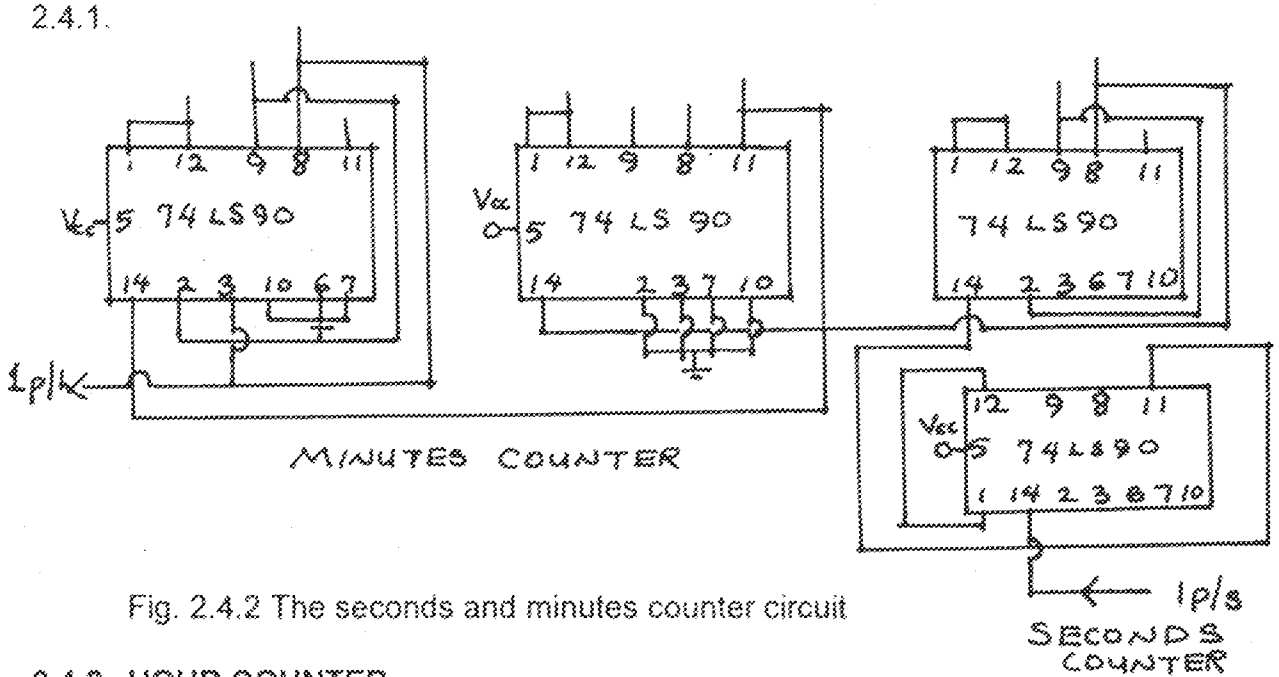


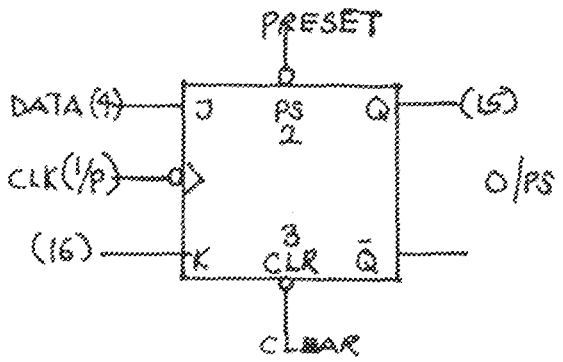
Fig. 2.4.2 The seconds and minutes counter circuit

2.4.2 HOUR COUNTER

The hours counter is slightly different. It has the 7490 IC as a decade counter in the units position. The output of this counter is inverted by an IC inversion, to provide the unit hours reset so that at 12:59:59, the clock resets to 01:00:00. In the tens of hours position however, instead of the 7490 IC previously used, a J K flip - flop (7476) is used. Since it is a 12 hour clock, this digit is only a 0 and 1. These two output states can easily be obtained using the 7476 IC which

is discussed below.

7476 IC



(i) Logic Symbol

MODE OF OPERATION	INPUTS					O/PS	
	ASYNCHRONOUS		SYNCHRONOUS				
	PS	CLR	CLK	J	K	Q	Q
Asynchronous set	0	1	x	x	X	1	0
Asynchronous reset	1	0	x	x	x	0	1
Prohibited	0	0	x	x	x	1	1
Hold	1	1	⊓	0	0	No change	
Reset	1	1	⊓	0	1	0	1
Set	1	1	⊓	1	0	1	0
Toggle	1	1	⊓	1	1	Opposite set	

(ii) Truth table X - irrelevant +ve clk pulse

Fig. 2.4.2

The logic symbol is in fig. 2.4.2 (i) above, showing the two asynchronous input (preset and clear) and the synchronous input J and K data clock inputs and the customary Q and Q outputs. Also the detailed truth table is shown in fig. 2.4.2 (ii). The asynchronous inputs are activated in the first three lines of the truth table overiding the synchronous inputs. When both asynchronous inputs (PS and CLR) are disabled with a 1, the synchronous inputs can be activated. W a 0 is applied to the clear input, the flip-flop resets. This feature is used in resetting the hour counter.

connected to the clear input of the 7476 the clear input is active and therefore the flip-flop reset to give a 0 output at the Q output of the 7476.. This reset input of the 7490 are also connected to the output of the 7411 which is at logic 1 this reset the 7490 counters back to 00. However, there is an active low inverter at the QA output which is activated and therefore there is a count of 1 on 7490. The hours counter therefore resets from 12hous to 01 hours.

2.5 THE DECODER SECTION

In digital electronics, all operations are carried out in binary from. The information at the output of the counter are in binary form therefore, it is necessary to find a way of converting this information in binary to a form suitable for a man to interpret and a circuit required for this purpose is known as a "DECODER".

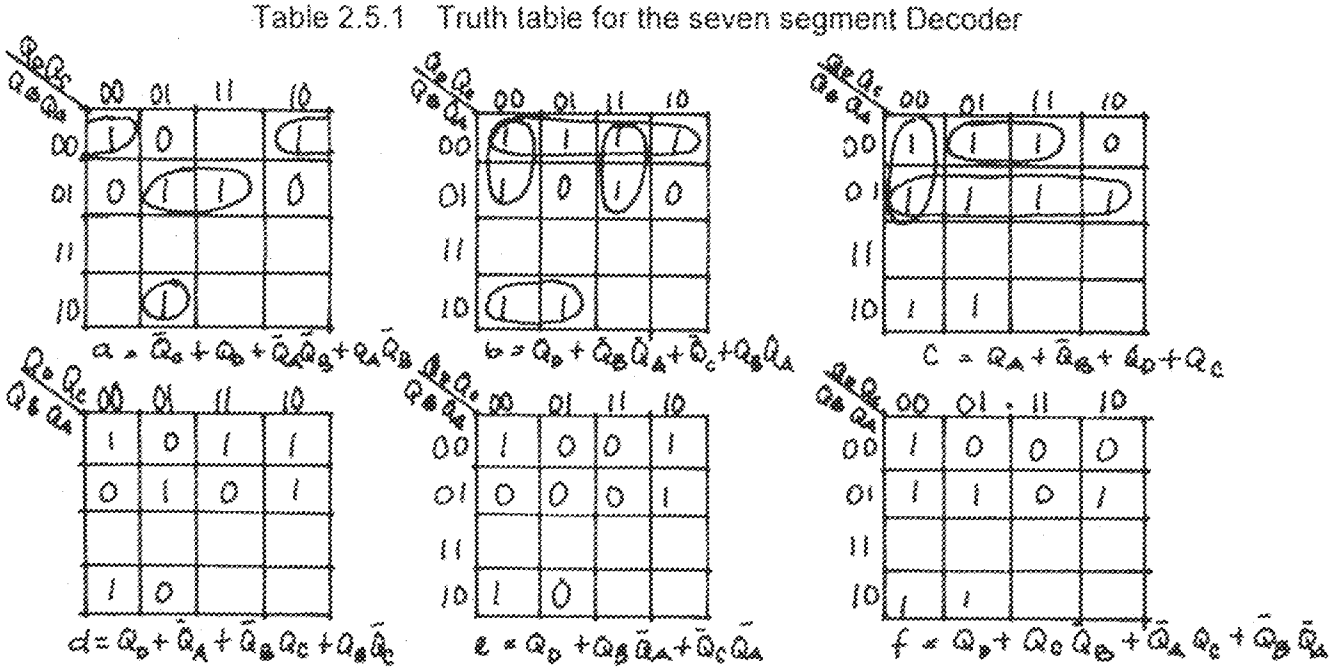
A DECODER: A decoder is a combinational logic circuit that converts binary information from n-input lines to a maximum of 2^n unique output lines. If the n-bit decoder information has unused combinations as is the case with the special decoder used for this project, the decoder output will have less than 2^n outputs. This decoders are refered to as n – to - m line decoders where m is less than or equal to 2^n.

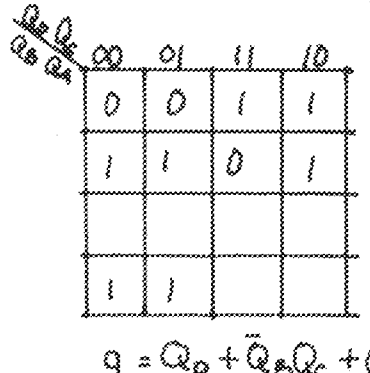
A seven segment decoder is used for this project. It is a 4 - to - 7 lines decoder. It has four inputs and seven outputs. These outputs are used to drive a seven segment display.

2.5.1 DESIGN OF A SEVEN SEGMENT DECODER

DENARY DIGIT	INPUTS				SEGMENT (ON=1)						
	Q0	Qc	QB	QA	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	1	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

Table 2.5.1 Truth table for the seven segment Decoder





2.5.2 CHOICE OF DECODER/DRIVER IC

As it can be seen in fig. 2.5.1, if one is able to implement this circuit using single scale integrated circuit, the number of components required is enormous. For example, this project required six seven segment decoders. If six of such circuit are to be implemented at the end of the day, the cost of production would be very high. Therefore, it would be wiser to go for circuit that is less costly and most effective and such circuit comes in a medium scale integrated circuit e.g 74LS47 decoder. It is a decoder/driver used to drive a seven segment display in this project.

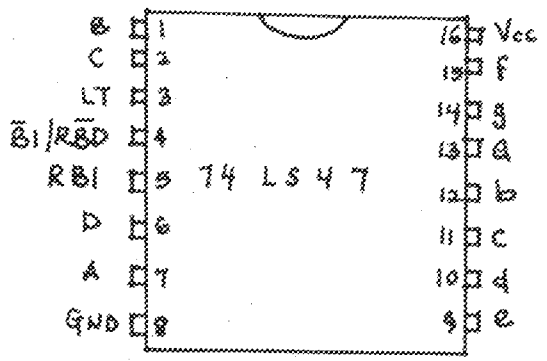


Fig.2.5.2 A seven segment Decoder (74LS 47)IC.

The figure shown above 2.5.2 is a 4 - to - 7 line decoder. It has four data inputs, A., B, C and D and seven active low outputs a, b, c, d, e, f, and g. These outputs. If a binary seven, A = 1, B = 1, C= I and D = O are present at the data inputs the output a , b, c and g would be at an active low since the display used in this project is a common-anode, only the segments to which these outputs are connected (a,b,c and g) are turned ON, therefore a decimal seven is then displayed.

2.6 DIGITAL DISPLAY OR READOUT

The display employed in this project is the seven segment display which is widely used as a readout for modern digital equipment.

There are three types of seven-segment display. These are

(i) Light emitting diode (LED)

(ii) Liquid Crystal display (LCD) and

(iii) Gas discharge display (GDD).

However, the seven-segment indicators in this project are basically Red light emitting diodes (LED) constructed on a veroboard in a geometrical pattern, dipicting the shape of decimal numbers from 0-9 depending on which segment is selectively illuminated as shown in the figure 2.6 below. The LED was chosen because it was cheap and available in the market.

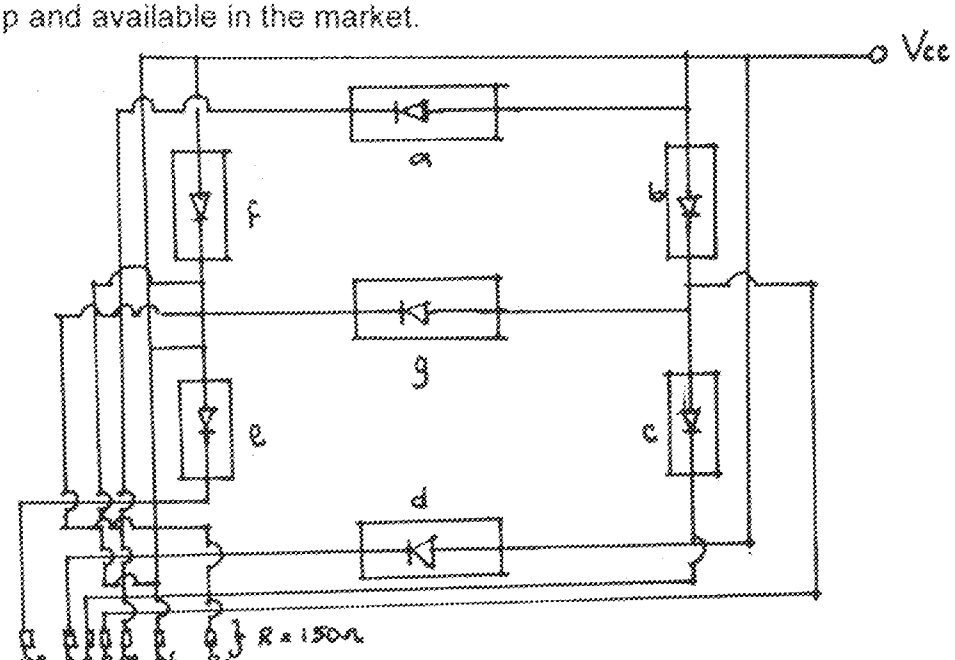


fig. 2.6 Red Colour Seven Segment Display.

The LED seven -segment is a common-anode display in which all anodes are connected together while the cathodes are independent as it is shown in fig 2:6.

To operate the LED display, all anode terminals must be supplied with positive voltage. The current flowing through each diode must be limited to about 20mA which is the maximum amount of current that must pass through each for safety. Therefore, in order to prevent current passing through these diodes, a current limiting resistor must be introduced in series with each diode at their respective cathode.

2.6.1 CALCULATING THE VALUE OF THE CURRENT LIMITING RESISTOR FOR THE SEVEN SEGMENT, LED DISPLAY

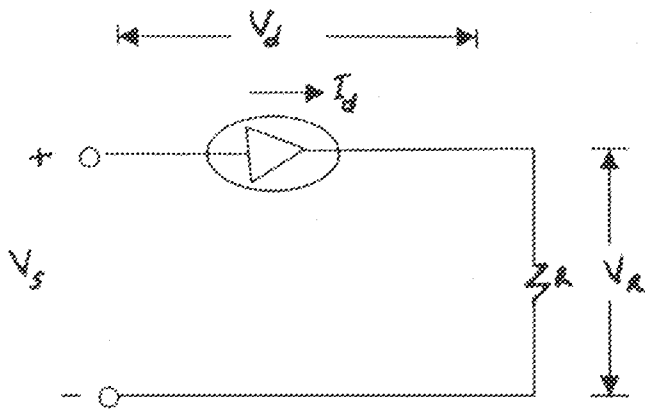


Fig.2.6.1(ii)

As it is shown in the circuit above (fig 3.6.1(ii)). The range of the voltage drop in the diode is $1.0 \leq Vd \leq 3.0$

Where Vs (supply voltage) = 5V

Id (diode current) = 20mA.

(a) For Vd (min) of 1.0V

from,

$$V_s = V_d + V_R$$

$$V_R = V_s - V_d$$

$$= (5-1)V$$

$$= \underline{4V}$$

Thus,

$$V_R = I_d R_L$$

$$R_L = \frac{V_R}{I_d} = \frac{4}{20 \times 10^{-3}}$$

$$= \underline{200\Omega}$$

(b) For V_d (max) of 3V

from,

$V_s = V_d + V_R$

$V_R = V_s - V_d$

$= (5-3)\ V$

$= \underline{2V}$

Thus,

$V_R = Id\ R_2$

$$R_2 = \frac{V_R}{I_d} = \frac{2}{20\times10^{-3}}$$

$= \underline{100\Omega}$

Therefore, the range of the value of limiting resistor is

$R2 \leq R \leq R1$

$100\Omega \leq R \leq 200\Omega$

$\therefore$ $R = 150\Omega$ was chosen.

2.7.0 THE POWER SUPPLY UNIT

In order to remove the stress from the power supply unit, this project design requires a dual voltage supply of + 5v. This was done because the total current consume by the whole circuit is more than IA and therefore two 5V IA (7805) regulator were connected in parallel so that the two of them now share the total current being drawn by the circuit together according to the Kirchoff's current law. The connection of the power supply is as shown in fig. 2.7.

The circuitry consists of a 220v/12v transformer whose outputs are fed into the diode rectifier to produce a dc voltage output. Some capacitors of specified capacitance values were used to remove ripples by way of fluttering. The two 7805

Ic voltage regulators were connected in parallel and used to produce constant dc voltage supply of +5v and +5v respectively which one of them is required to power display, decoder and accumulator sections while the second + 5v is used to power time base and frequency divider sections.

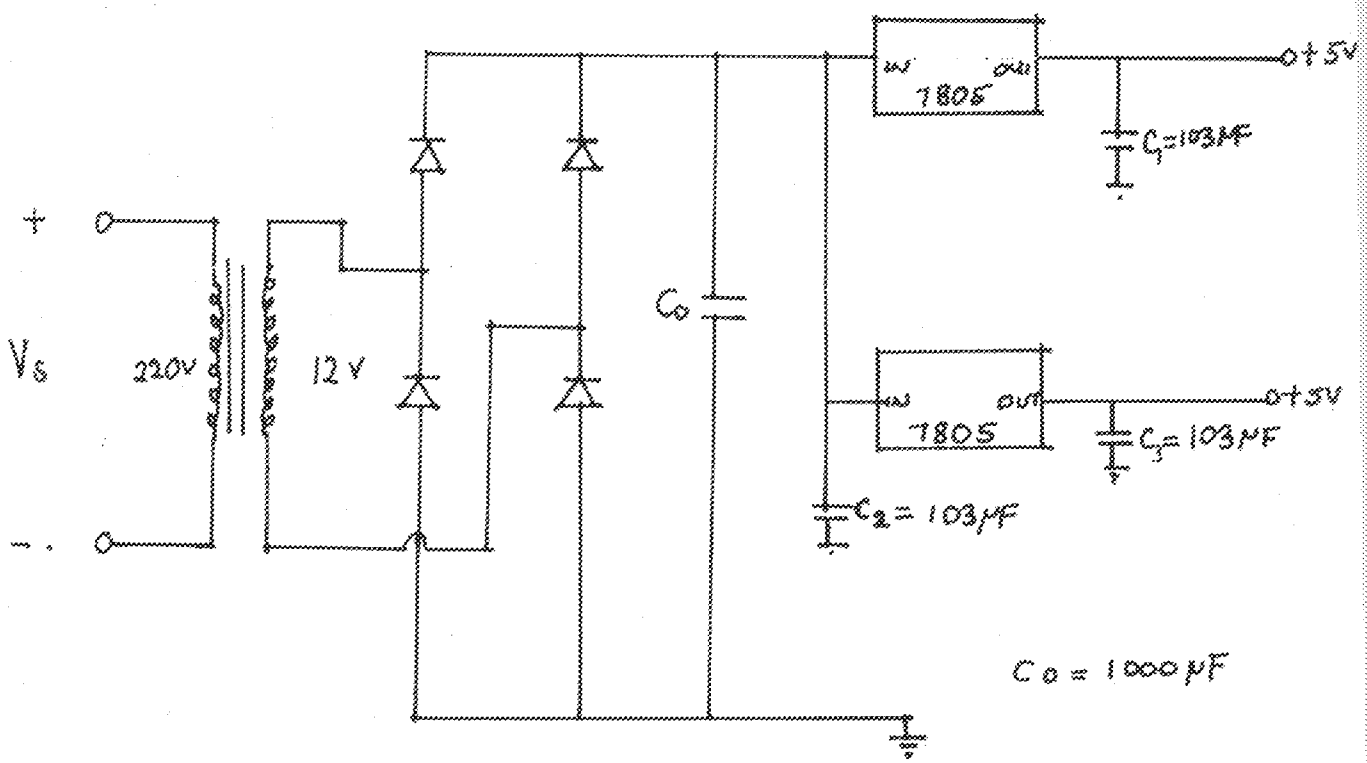


Fig 2.7.0

THE POWER CIRCUIT

CHAPTER 3

CONSTRUCTION TESTING, TROUBLE SHOOTING AND COSTING.

3.1 CONSTRUCTION

In the construction of each of the sections that make up the DIGITAL CLOCK, the design specification are strictly adhere to and the logic family used in the project is restricted to a particular one T.T.L, after considering the problems associated with the interfacing of different logics. However, the construction of each of the sections are discussed below.

A regulated power supply section was constructed on veroboard using transformer rating of 22ov,500mA (Primary), 12v (secondary) as shown in the fig. 2.7 of the chapter two feeding a bridge rectifier constructed by four1A general purpose diode and the output of this now filler by capacitor Co, which is 1000 µF . In this section two 5v, 1A regulator are used and they were connected in parallel because the total current consume by the, while circuit is more then 1A, and with the two of them in parallel world share it according to the kerchiefs current law. the output of one would supply both decoder and LED section while the second one would supply the rest section .capacitors C1,C2 and C3 are used for something stage in the circuit.

The pulse generator was constructed using 555 time as an AS TABLE MULTIVIBRATOR with R1 =680Ω, R2 = 6.80kΩ and a capacitor of 0.1µF as calculated in chapter 2 giving output of 1000pulse per second

The frequency divider section was constructed using three decade counter which were connected in series with the final output of 1 pulse per second

The count accumulator Were constructed using decade. Counter .The unit

of second and minutes are constructed by taking its input from pin 14 and output from pin11 with pin 2,36,7and 10 grounded. The tens of second and minute are constructed by taking its input from pin14 and output from pin8 with pin 10, 6 and 7 grounded. pin 2 and 9 connected together as shown in chapter two.

The unit of hour was constructed with a decade courter with an inverter at pin 12output while the tens of hour was constructed using a flip-flop, AND gate and inverter.

The decoder/driver and display section were constructed using the output of the court accumulator as its own input and a limiting resistors of 150Ω were used to limit the current from output of the decoder\driver to the sever-segment display which were constructed using the light emitting-diodes.

However, the stages were arranged in such a way that the output of one stage serves as the input to the other stage.

3.2 TESTING

Each of the section were first tested one after the other on a bread broad and considerable time was given to each module under test to respond as desired so as to be sure of its reliability.After the breadboard testing, each module were the disconnected from the breadboard and then transferred to the veroboard for permanent soldering. And proper soldering techniques were carefully observed.

However, the final soldering of the entire circuit, was then tested section by section by multi-metre to make sure that they are working as desired.

3.3 TROUBLESHOOTING

It is desired that in improving the maintenance culture, one should also be able to rectify some simple faults which might develop in the digital clock.

To this end , some common faults which could easily develop in the clock are

enumerated and simple suggestions on how to go about rectifying them enlisted in the table below.

FAULT (S)	POSSIBLE CAUSE (S)/ SUGGESTION	TOOLS/EQUIPMENTS TO USE
Supply mains on, power supply not working	Fuse might have got burnt, or transformer burnt or any of the components in the power supply section. Carry out check on each of these as appropriate	Multi-meter, Oscilloscope, soldering iron, lead/sucker
Supply main On, power supply unit working but clock not working	Seven-segment LED indicator might have been burnt, counter might have failed, clock generator IC might have failed, study the detail circuit diagram and carry out fault tracing as appropriate	Multimeter, oscilloscope, soldering iron, lead/sucker, IC extractor and plier.

Table 3.3

3.4 COST ANALYSIS

This table gives the part list for the Digital Electronics clock and their cost. The list includes only those components used in the final production and excludes those that burnt or damaged during the course of production.

NO	DESCRIPTION OF COMPONENTS	QTY	UNIT PRICE (₦)	TOTAL COST (₦)
1.	Limiting resistors RI = 150Ω	42	7.00	294.00
2	Resistor RI = 680 Ω	1	8.00	8.00
3	Resistor R2 = 6.8kΩ	1	8.00	8.00
4	Capacitor C0 = 1000 μF	1	60.00	60.00
5	Capacitor C1 = 0.1 μF	1	40.00	40.00
6	Capacitor C2 = 0.01 μF	1	35.00	35.00
7	$C_1 = C_2 = C_3 = 103\mu F$	4	50.00	200.00
8		1	150.00	150.00
9	Transformer 220v/12v	1	100.00	100.00
10	500mA	1	80.00	80.00
11	7402 IC	5	100.00	500.00
12	7404IC	8	120.00	960.00
13	74LS47 IC	1	100.00	100.00
14	74 LS 90 IC	1	80.00	80.00
15	74 76 IC	2	100.00	200.00
16	7411 IC	2yrds	30.00	60.00
17	78 05 IC	6yrds	10.00	60.00
18	Connecting vires	4	20.00	80.00
19	Soldering lead	2	100.00	200.00
20	General purpose diode (1A)	1	30.00	30.00
21	Veroboard	2	30.00	60.00
	Push - button			
	Plastic casing			
			TOTAL	**3,305.00**

CHAPTER FOUR

DISCUSSION, SUGGESTION AND CONCLUSION

4.1 DISCUSSION AND SUGGESTION

The project is aimed at design and construction of a clock with a high degree of accuracy and one that is less tedious in its use for measurement. This aim was achieved though with some technical difficulties.

Problems were encountered in the area of getting an accurate pulse frequency using the 555 timer IC. It was not easy to get one pulse per second from the 555 timer that was why the time base was made to generate 1000 pulse per second and this was divided using three decade counters which their total output gave 1 pulse per second which is the required pulse for counting by accumulator. Moreover, problem were encountered in the power unit section because the output of a regulator does not sustained the power consume by the circuit, therefore, the problem was solved by using two regulators in parallel in which the output of one regulator will serve decoder and display module while the second will serve the rest of the circuit. Also heat sink is used for the regulator IC to conduct the heat away and LED are used in such away that they are arranged in numerical order for the display circuit.

Besides, in the area of getting components for the project work also some difficulties were met. When some components gets burnt at the course of construction, it becomes very difficult and costly to get then replaced and this waste a lot of time and causes delay in the construction.

However, after the satisfactory job that we have done the possible future improvement on the project are as follows:

(i) Incorporation of the mode select switch to reset the hour and minute digits.

(ii) The clear reset switch or button may also be incorporated.

(iii) The alarm circuit which will operate hourly.

Also going by my experiences during the cause of designing and construction of this project, I hereby suggests:-

that the university or department should embrace the culture of helping and assisting students in getting the components needed for their project work and also they should try to relief students financial wise on their project.

Besides, I also suggest, that students of the department should be made to start embarking on mini-project work from 300 level upwards. This will go along way in exposing and preparing the electrical students for their final year project.

Finally, the department should set up more laboratory practical in electronics for students and a film show (Documentary Film) on electronics should always be shown for students.

4.2 MAINTENANCE

In engineering profession, maintenance of engineering equipments (whether in form of tools or measuring instruments) is very necessary and important since continuous and constant maintenance of equipments leads to increased life span of such equipments and hence higher profitability.

The digital clock in this sense is unarguably on engineering equipment used for measuring time. Hence, the need to take good care of it is mandatory to generate its durability.

4.2.1 MAINTENANCE CULTURE TO BE OBSERVED ON THE DIGITAL CLOCK

1. Always place the digital clock at moderately ventilated locations to prevent overheating, to aid proper heat sinking by transformer and other heat generating components.

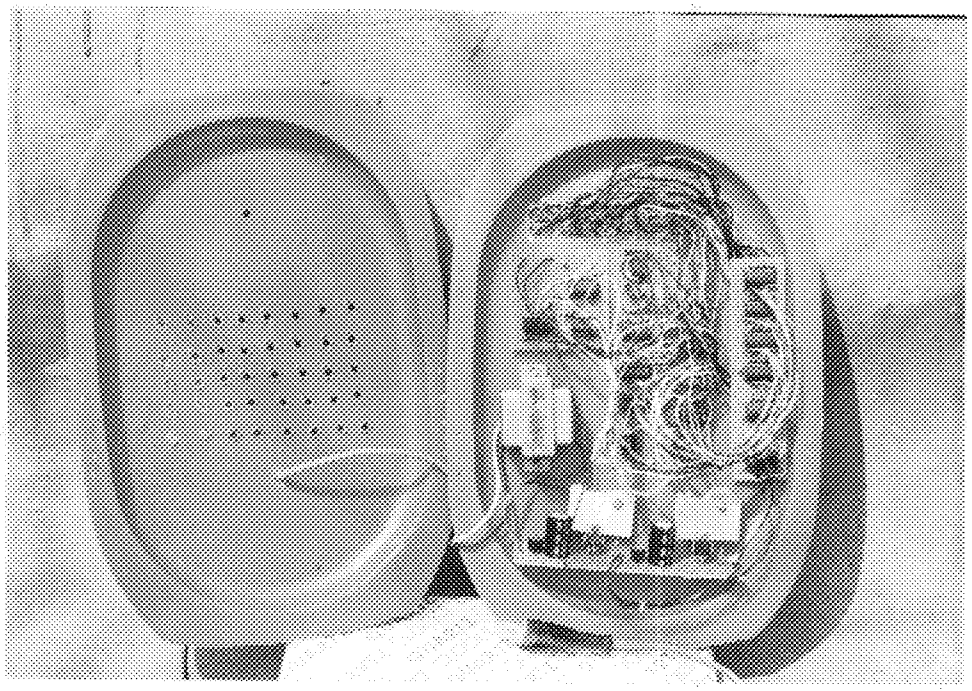
2. Disallow anything liquid, moisture or dirty air from entering into the housing or casing of the clock as electronics components do not compatible with them.

3. Always handle properly when moving the clock to another location to prevent the clock from falling which could lead to the malfunctioning or complete damage of the clock.

4. Always ensure that the power cord does not kink as kinking could damage the cord and can cause short circuit.

4.3.0 CONCLUSION

The aim of this project has undoubtedly been achieved though some discrepancies is always occur when the clock is connected to the power supply and this is due to false triggering of digital IC used and this could be overcome by allowing the system to attain a steady state. That is to say that the required circuit has been designed, constructed and it is working satisfactory. The design was carried out by the knowledge acquired from Electronic and Digital courses offered in our department as well as industrial training.



(i) COMPONENTS LAYOUT

(ii) FINAL CASING OF THE PROJECT.

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