

DESIGN AND CONSTRUCTION OF ELECTRONIC CODE LOCK FOR DOOR

BY

MOHAMMED SALAMI

1998/7223EE

**DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING**

**SCHOOL OF ENGINEERING AND
ENGINEERING TECHNOLOGY**

FEDERAL UNIVERSITY OF TECHNOLOGY

MINNA, NIGERIA

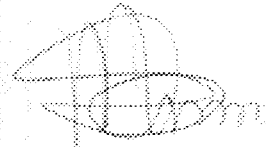
NOVEMBER 2004

DEDICATION

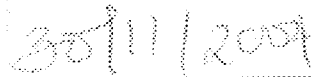
To God the almighty, the giver of life, the giver of wisdom and understanding through whom I breath

DECLARATION

I hereby declare that the project was wholly designed and constructed by me under the able supervision of Engineer Asula, Department of electrical and computer engineering, Federal University of Technology Minna.



(sign of student)



Date

CERTIFICATION

This is to certify that this project work title "Design and construction of Electronic Combination lock for door" was carried out by Mohammed Salami (98/7223EE) for the award of Bachelor of Engineering (B>ENG) Degree in Electrical and Computer Engineering; Federal university of technology Minna.

Engr. Asula

Project supervisor

Asula 15.12.2007

Sign & Date

Engr. M. D. Abdullahi

Head of Dept.

.....
Sign & Date

.....
External Examiner

.....
Sign & Date

ACKNOWLEDGEMENT

I am especially grateful to my parent Mr. & Mrs. Salami, who have been giving me much appreciated support, and for believing in me. I am most indebted to them special thanks goes to Kamali Salami, my brother, Bukky Salami, Banke Salami and Medina Salami, my sisters and my sibling nieces and nephews. Gratitude is also expressed to my project supervisor, Engr Asula whose correction supervision and co-operation has made this work a success. My grateful thanks go to my H.O.D Engr. M. D. Abdullahi and all the lecturers in Electrical and Computer Engineering department for their influence and import in my academic life.

Finally to my friends and colleagues at the university and all my course mates for their support. I am grateful once again to my supervisor for his suggestions and painstaking work in editing the project report and for his professional suggestions in the construction of the project.

ABSTRACT

This project titled "Combination lock" is designed to provide dependable security lock system in order to deny unauthorized person access to a specific room(s) where it is installed. It allows an unlock code of eight digit which makes it absolutely impossible to guess.

To accomplish the aim and objective of the projects Cmos ICs CD4022B, IN914a speed diode, BS170 N-channel enhancement mode field effect transistor and other associated components were used.

CD4022B is used as the basic component of the counter unit whose decoded outputs are used via switches to form the keyboard unit. CD4022B has eight decoded outputs and consequently, the keyboard composed of eight switches, hence eight codes.

IN914A speed diode and BS170 N-channel enhancement mode field effect transistor are one each both connected to the CD4022B counter reset and clock terminals respectively.

TABLE OF CONTENT

TITLE PAGE.....	i
DEDICATION.....	ii
DECLARATION.....	iii
CERTIFICATION.....	iv
ACKNOWLEDGEMENT.....	v
ABSTRACT.....	vi
CHAPTER ONE	
GENERAL INTRODUCTION	
1.1 INTRODUCTION.....	1
1.2 AIM AND OBJECTIVE.....	1
1.3 LITERATURE REVIEW.....	1
1.4 PROJECT OUTLINE.....	3
CHAPTER TWO	
DESIGN ANALYSES AND PRINCIPLE OF OPERATION	
2.1 BLOCK DIAGRAM.....	4
2.2 DESIGN ANALYSIS.....	4
2.3 CIRCUIT DIAGRAM.....	7
2.4 THEORY OF OPERATION.....	8
2.5 COMPONENTS/COMPONENT DESIGN.....	8

CHAPTER THREE

CONSTRUCTION, TESTING AND RESULT

3.1	CONSTRUCTION.....	34
3.2	TESTING.....	35
3.3	RESULTS.....	35
3.4	DISCUSSION OF RESULTS.....	36

CHAPTER FOUR

CONCLUSIONS AND RECOMMENDATIONS

4.1	CONCLUSION.....	37
4.2	RECOMMENDATION.....	37
	REFERENCE.....	38
	APPENDIX A:.....	39
	APPENDIX B:.....	40

CHAPTER ONE

1.0 GENERAL INTRODUCTION

1.1 INTRODUCTION

In recent times the use of key locks for doors has been unreliable with various nefarious acts of illegal intruders which includes taking impression of key or by use of so called master key.

Consequently, there has been a need to fabricate a lock mechanism that will be almost absolutely reliable and serves as check for unauthorized users. This security objective is characterized by the use of electronic lock that is authorized user friendly and it is convenient. Thus the design and construction of electronic is imperative.

1.2 AIM AND OBJECTIVE

This project design and construction of "Electronic Combination Door Lock", Is aimed at providing reliable security lock to meet the security specification and requirement of domestic, office and public utilities security standards.

1.3 LITERATURE REVIEW

Lock is a device that secures such things as a door of a house or a cabinet, a lid of brief case or other luggage, and the action of an ignition system by means of a bolt or latch that can be released by a mechanical, hydraulic, or electrical/electronic (actuator).

The use of the locks extends back to the beginning of recorded history. The oldest know mechanically functioning lock was an Egyptian door lock use about 2000BC. A

forerunner of the modern pin-tumbler security, the lock consisted of a vertical wooden housing containing several loose wooden pegs of different lengths. The early Greeks utilized the first keyhole by fastening the wooden lock and staple to the inside of the door. Both had the disadvantage of not long lasting as they were wholly made of wood.

The Romans fabricated the first metal locks with later improvement by Robert Barson, an English man in 1778 and Linus Yale, Jr., an American in 1861. In the 20th century, as machine tools and manufacturing methods became more sophisticated, locks were produced with closer parts tolerances, resulting in better security.

Many types of locks appeared in 20th century. Locks now are either key operated (opened) and keyless. Narrowing down to the key locks, in late 20th century, electromechanical locks were developed to trip electrical circuit as in automobile ignitions. Unfortunately, the use of key locks is unreliable with the use of "master keys" by illegal intruders.

The keyless locks are the most modern locks, they were first invented and made popular in late 20th century, the keyless locks are remote control lock,"security card" operated, and electronic lock.

Interestingly, electronic lock is a lock designed to respond to an electronic logic signal mechanism, with a digit sequence counter performing the function of the key. This is the exact attribute of this project.

This project (electronic lock) solves the problems associated with other keyless locks. The lost or breaking of the portable card of the card operated door lock is a big problem. Similarly, access to the use of the door is denied if there is a lost, theft or misplacement of the remote control of the remote control lock.

The digit sequence counter employed in this project is the octal decimal counter CD4022BCOMS IC that allows eight characters as the code. This undoubtedly reliable IC will achieve the set objective of security, reliability and fast response.

1.4 PROJECT OUTLINE

In this first chapter, a general introduction to the project work is given. The aim and objective of the project are highlighted; literature concerning the project was then reviewed.

Chapter two deals with the system design and analysis

Chapter three covers the construction of the system, testing, results and discussion of the result

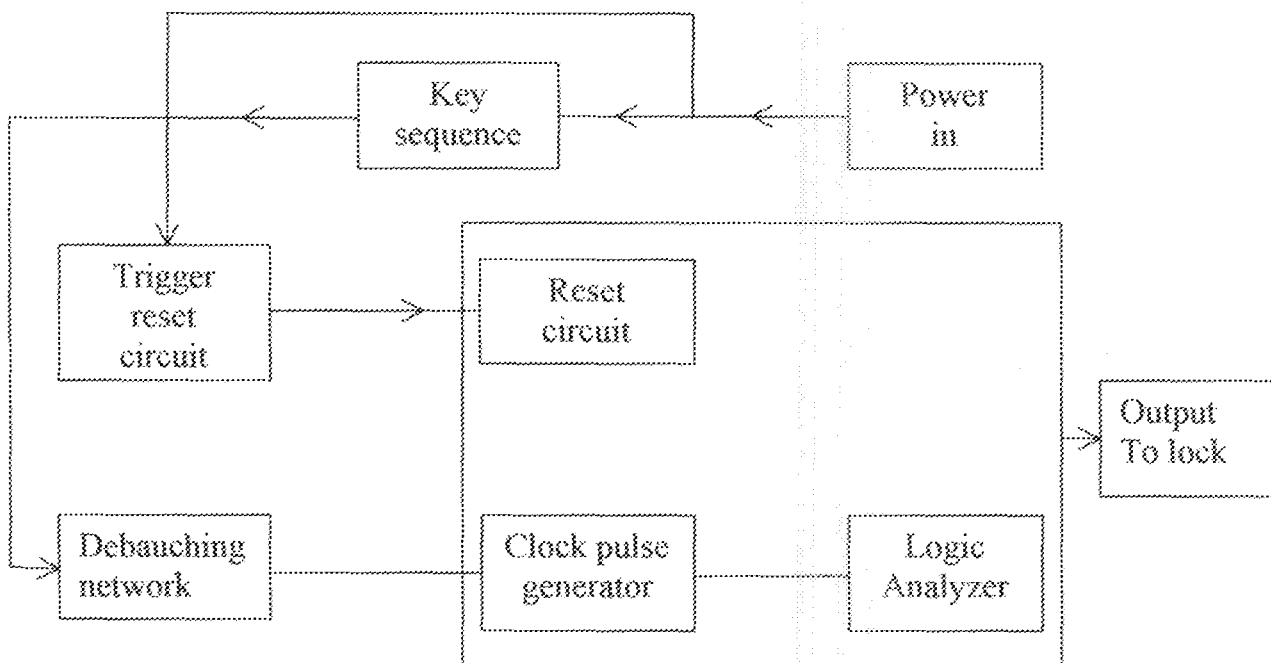
Chapter four gives the conclusions and recommendations.

Appendix and reference lists are provided at the end of the report.

CHAPTER TWO

SYSTEM DESIGN ANALYSIS AND PRINCIPLE OF OPERATION

2.1 BLOCK DIAGRAM



2.2 DESIGN ANALYSIS FOR COMBINATION LOCK

POWER IN

Power is feed into the counter via a resistor and a capacitor to reset the counter and also to power the clock circuit.

KEY SEQUENCE

The first key on the combination when pressed causes the counter to reset, which is cleared to the zero point. The key has to be pressed in the ascending order of the output. That is, the key connected to the output pin Q_0 of the counter must be pressed first followed by that connected to Q_1 , then Q_2, Q_3, \dots

TRIGGER RESET CIRCUIT

The trigger reset circuit is made up of a resistor and a capacitor that resets the counter by outputting a high to pin 15 of the counter which is the reset pin.

DEBOUNCING NETWORK

It is made up of the BS170 transistor, a resistor and a capacitor. When pressing the first key correctly activates the network, it feeds pin 14 of the counter with a high input.

RESET CIRCUIT

The reset circuit is activated when the wrong is key pressed, thus, bringing the circuit to its starting state.

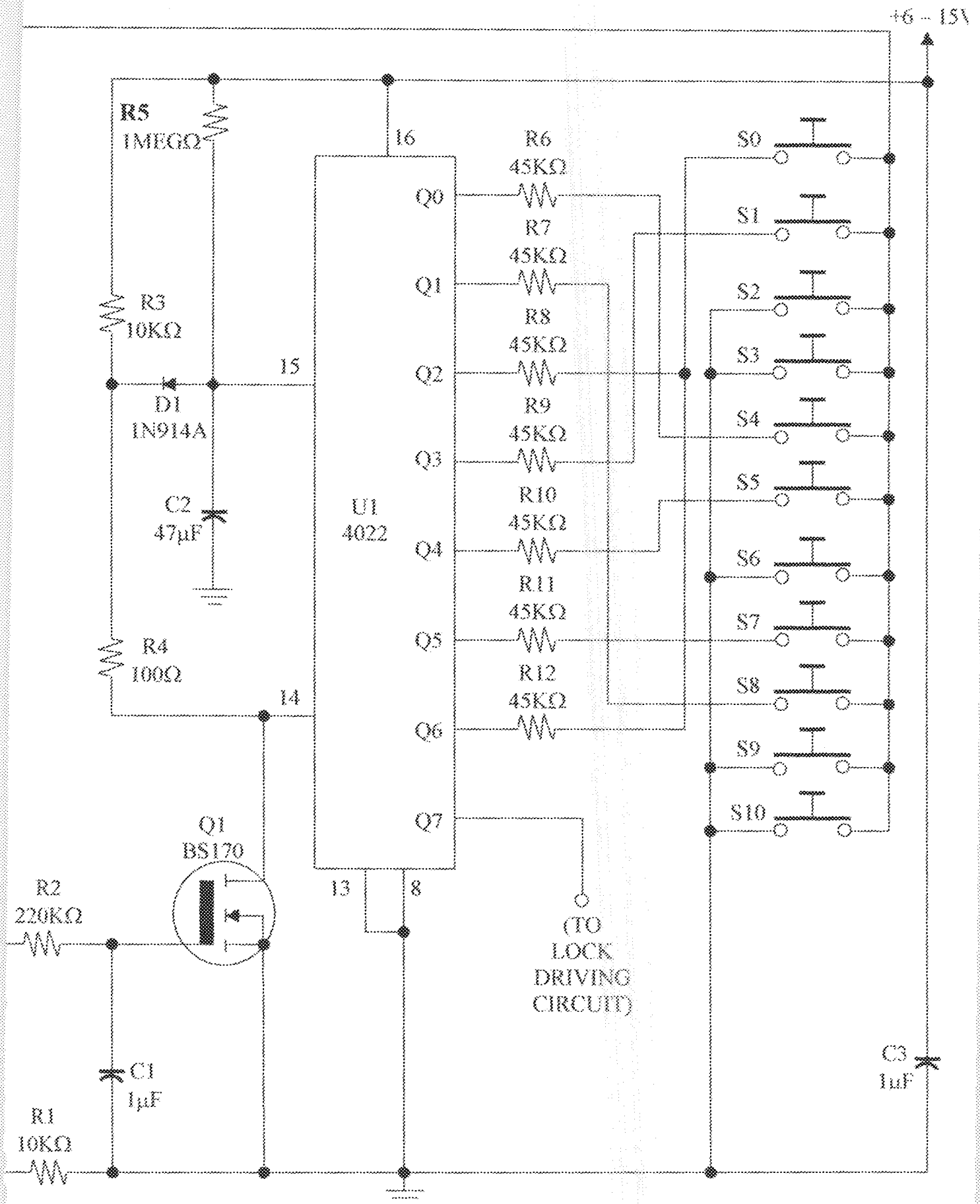
CLOCK PULSE GENERATOR

This is a part of the counter that takes its input from pin 14. When a high is inputted, a clock cycle is started.

LOGIC ANALYZER

It is a part of the counter too. When the correct key sequence are pressed during the clock cycle generated by the clock pulse light. When the last key is pressed, the 8th output of the counter goes high for about 4 seconds, these is connected to the relay driving circuit to control the opening of the door under lock.

2.3 CIRCUIT DIAGRAM



2.4 THEORY OF OPERATION

The heart of the circuit is a 4022 octal counter. When first powered up, C_2 is charged via R_5 , so the reset input of the counter is kept high. That causes output Q_0 to go high while all other outputs are low. With the switches wired as shown, when S_4 is pressed, the BS170 is switched on via debouncing network R_2/C_1 , and U1 receives a clock pulse. Also C_2 is discharged via R_4 and D_1 , removing the reset signal of the counter, allowing it to advance. The time that can lapse before the next key is pressed. The above cycle is therefore repeated only if S_8 (connected to the Q_1 output) is pressed in time. When all keys have been pressed in time and in correct order, Q_7 goes high for about 4(four) seconds to drive the "unlock" circuit (e.g., a relay driver for an automatic door opener). A builder can change the code by reviewing the switches. The code for the lock shown in the diagram is 4-8-0-1-5-7-6. However, the 4022 octal counter can be replaced by a 4017 divide-by-10 counter. That will make it possible to add two more digits to the combination.

2.5 COMPONENTS AND COMPONENT DESIGN

BATTERY

Electrical consist of electromagnetic cell in which chemical energy is converted to electrical energy.

Each cell has a negative electron, an electrolytic solution and electrodes in separate places in a suitable container.

The electrode is in a reduced state while the positive electrode is in an oxidized state. When the cell is operated the negative electrode oxidizes and the positive becomes

reduced. The negative electrode yield electron to an external circuit and the positive electrode accept electrons from this circuit. Thus the electron flows from the negative electrode to the positive electrode, a direction contrary to what is conventionally known as the "Directionally of the current" is carried through the battery by ions of the electrolytic solution. Usually each electrode is made up of joining a number of plates in parallel. The electrical capacity is proportion to the number.

There are two types of electric cell:- (I) Primary cells

(II) Secondary cell.

Chemical energy is converted to electrical energy and the process cannot be reversed. In secondary cell inter connection of chemical and electrical energy can be achieved in repeated circuit. Because of the reversibility, secondary batteries are also called storage batteries.

There is a different type of battery cell called: -lead-acid battery, nickel ion batteries, zinc-acid battery because it is easily available.

LEAD-ACID BATTERIES

Lead-acid batteries are manufactured in various designs to suit different application, such as aircraft automotive, low discharge service.

A lead-acid cell consist of essential of positive plates containing lead peroxide and negative plate containing pure lead immersed in an electrolyte of dilute acid.

CARE AND OPERATION OF BATTERIES

The essential feature of general care of storage batteries is simple and few, but they are essential

- (a) keep the battery clean and dry
- (b) Add water(which is proving by manufacturer)from time to time to keep the level of the electrolyte alive.
- (c) Never add electrolyte or acid except to replace loss ones

RESISTORS

Resistors are used to limit the current in a circuit. When choosing a resistor, three factor are considered apart from the value.

- (1) *THE TOLERANCE*:- The exact value cannot be guaranteed by mass production method, but this is not a disadvantage because in the electron circuit the value of resistors are not critical. A resistor with a stated value of 100Ω and a tolerance of $\pm 100\%$ could have any value between $90-100\Omega$
- (2) *POWER RATING*:- This is the maximum current which can be developed in a resistor without damage occurring by heating for most of electron circuit 0.25 or $5w$ rating are adequate
- (3) *STABILITY*:- It is the ability to keep the value with change of temperature and age.

CAPACITOR

Capacitors store electronic charges. Basically it consist of two plates separated by an insulator called dielectric.

CHARGING

When connected to a battery, the positive of the battery attracts electrons from one plate end of the capacitor and the negative of the battery repels electron to the other plate. Positive charges (deficit of electron) builds up the one plate end and an equal negative charge(excess of electrons) build upon the other plate.

During the period of charging, there is a brief flow of electron round the circuit between the two plates. Charging stops when the potential difference (P.D) between the two plates are equal (and opposes) to the E.M.F of the battery. This process take time i.e the response of a capacitor to a change of potential difference is not immediate.

When choosing a capacitor two factors to be considered apart from it's value and tolerance are:

- (1) **The working voltage:** It is the maximum voltage it can withstand before the dielectric breaks down (it is mark on it) and,
- (2) **The leakage,** though it should be small.

DIODES

A diode is a two-terminal device consisting of a P-N junction formed from either a Germanium or Silicon crystal.

The P- and N- type regions are referred to as anode and cathode respectively. The arrowhead in the circuit symbol, indicates the conventional direction of current flow when forward-biased. It is the same direction in which hole flow takes place.

A P-N junction diode is a one way device offering low resistance when forward-biased and behaving almost as an insulator when reverse-biased. Hence, such diodes are

mostly used as rectifiers i.e. for converting alternating current to direct current. The different types of diodes are, Small signal diode, Zener diode, Tunnel diode, Varactor diode, PIN diode, Schottky diode, Step Recovery diode, Gunn diode, IMPATT diode, Light Emitting diode, Photo diode e.t.c.

APPLICATION OF DIODES

- (1) As power or rectifier diodes. They convert ac current into dc current for dc power supplies of electronic circuits.
- (2) As signal diodes in communication circuits for modulation and demodulation of small signals.
- (3) As Zener diodes- in voltage stabilizing circuits.
- (4) As Varactor diodes- for use in voltage controlled tuning circuits as may be found in radio and TV receivers. For this purpose the diode is deliberately made to have a certain range of junction capacitance.
- (5) In logic circuits used in computers.

HIGH-SPEED DIODES

The 1N914 is of two types, the 1N914A and 1N914B. They are high speed switching diodes fabricated in planar technology, and encapsulated in a hermetically sealed leaded glass. Either of the two is suitable for project.

FEATURES

- Hermetically sealed leaded glass SOD27[D0-35] package
- High switching speed [maximum of 4ns]
- Continuous reverse voltage [maximum of 75V]
- Repetitive peak reverse voltage [maximum of 100V]
- Repetitive peak forward current [maximum of 225mA]

APPLICATIONS

- High-speed switching.

LIMITING VALUES

The limiting values stated are in accordance with the absolute Maximum Rating System [IEC 6S134]

SYMBOL	PARAMETER	CONDITIONS	MINIMUM	MAXIMUM	UNIT
V_{RRM}	Repetitive peak reverse voltage		-	100	V
V_R	Continuous reverse voltage		-	75	V
I_F	Continuous forward current	See fig.2	-	75	mA
I_{FRM}	Repetitive peak forward current		-	225	mA
I_{FSM}	Non-repetitive forward current	Square wave; $T_c=25^\circ\text{C}$ Prior to surge (see fig.4) $t_1=10\mu\text{s}$; $t_2=1\text{ms}$; $t_3=1\mu\text{s}$	-	4,1 & 0,5	A
P_{tot}	Total power dissipation	Temp = 25°C	-	250	mW
T_{stg}	Storage temperature		-65	+200	$^\circ\text{C}$
T_j	Junction temperature		-	175	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS

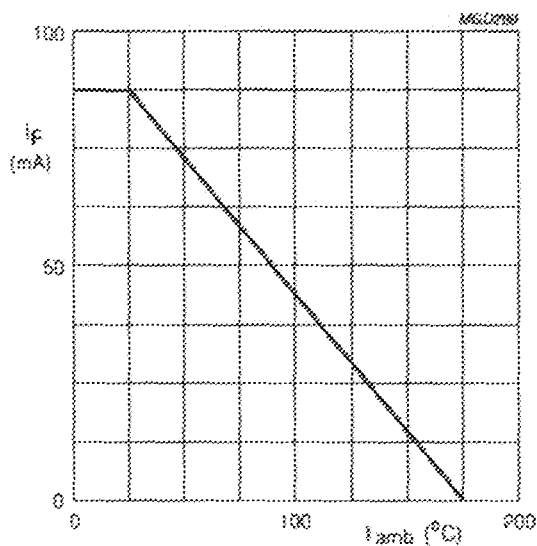
$T_j = 25^\circ\text{C}$

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_F	IN914A	$I_F = 10\text{mA}$	-	1	V
	IN914B	$I_F = 5\text{mA}$	0.62	0.72	V
	IN914B	$I_F = 100\text{mA}$	-	1	V
I_R	Reverse current	$V_R = 20\text{V}$	-	25	nA
		$V_R = 75\text{V}$	-	5	mA
		$V_R = 20\text{V}, T_j = 150$	-	50	mA
C_D	Diode capacitance	$F = 1\text{MHz}, V_R = 0$	-	4	pF
t_{rr}	Reverse recovery time	When switched from $I_F = 10\text{mA}$ to $I_R = 10\text{mA}$, $R_L = 100\Omega$; measured at $I_R = 1\text{mA}$	-	8	ns
		When switched from $I_F = 10\text{mA}$ to $I_R = 60\text{mA}$; $R_L = 100\Omega$; measured at $I_R = 1\text{mA}$	-	4	ns
V_S		When switched from $I_F = 50\text{mA}$; $t_r = 20\text{ns}$	-	2.5	V

THERMAL CHARACTERISTICS

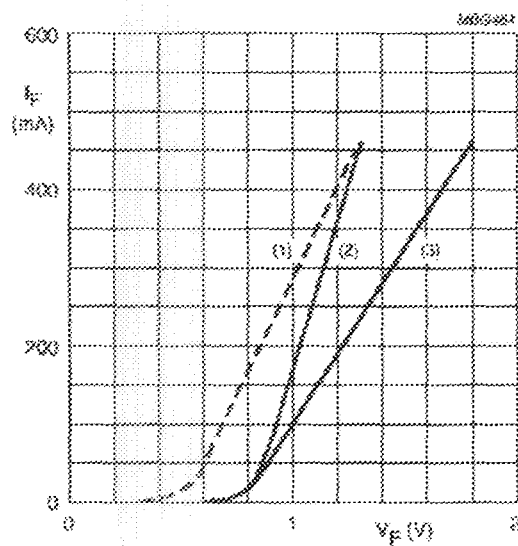
SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R_{th-j-p}	Thermal resistance to tie point	Lead length 10mm	240	K/W
R_{th-j-a}	Thermal resistance from junction to ambient	Lead length 10mm	500	K/W

GRAPHICAL DATA



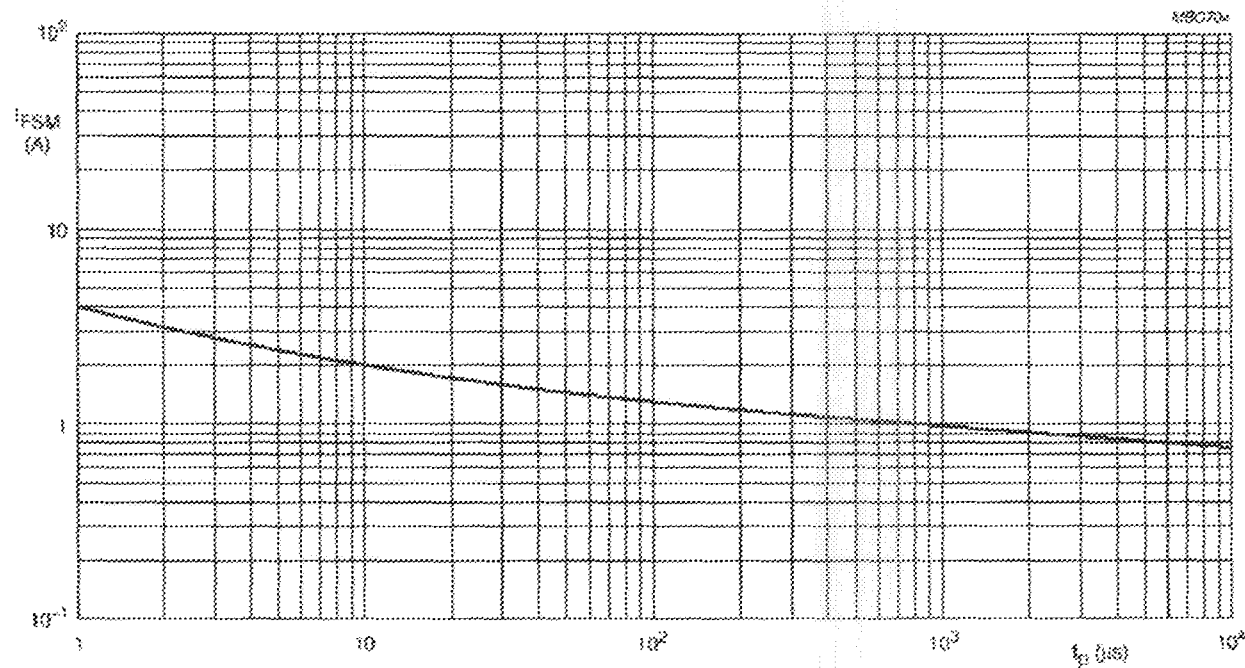
Device mounted on an FR4 printed-circuit board; lead length: 10 mm

Fig. 2 Maximum permissible continuous forward current as a function of ambient temperature.



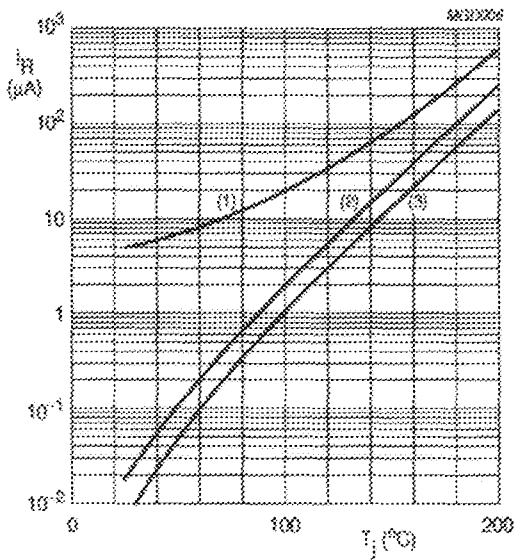
- (1) $T_j = 175^\circ\text{C}$; typical values
- (2) $T_j = 25^\circ\text{C}$; typical values
- (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 3 Forward current as a function of forward voltage.



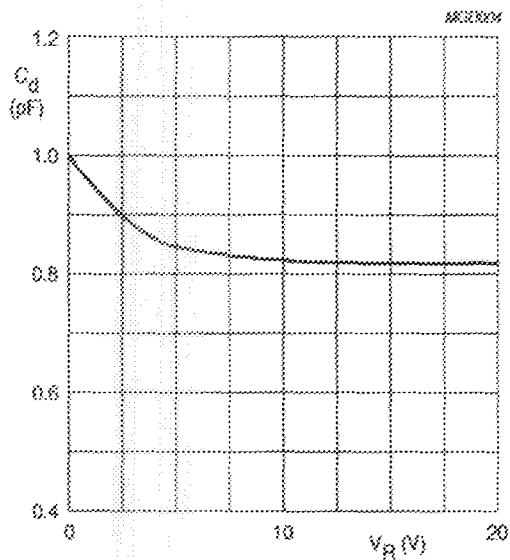
Based on square wave currents.
 $T_j = 25^\circ\text{C}$ prior to surge.

Fig. 4 Maximum permissible non-repetitive peak forward current as a function of pulse duration.



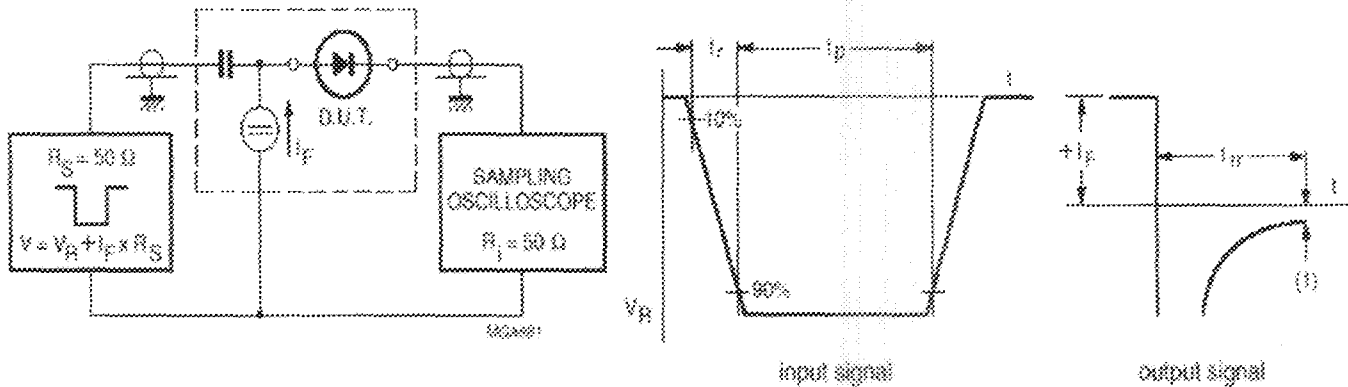
- (1) $V_R = 75$ V; maximum values.
- (2) $V_R = 75$ V; typical values.
- (3) $V_R = 20$ V; typical values.

Fig. 5 Reverse current as a function of junction temperature.



$f = 1$ MHz; $T_J = 25$ °C.

Fig. 6 Diode capacitance as a function of reverse voltage; typical values.



(3) $I_F = 1$ mA.

Fig. 7 Reverse recovery voltage test circuit and waveforms.

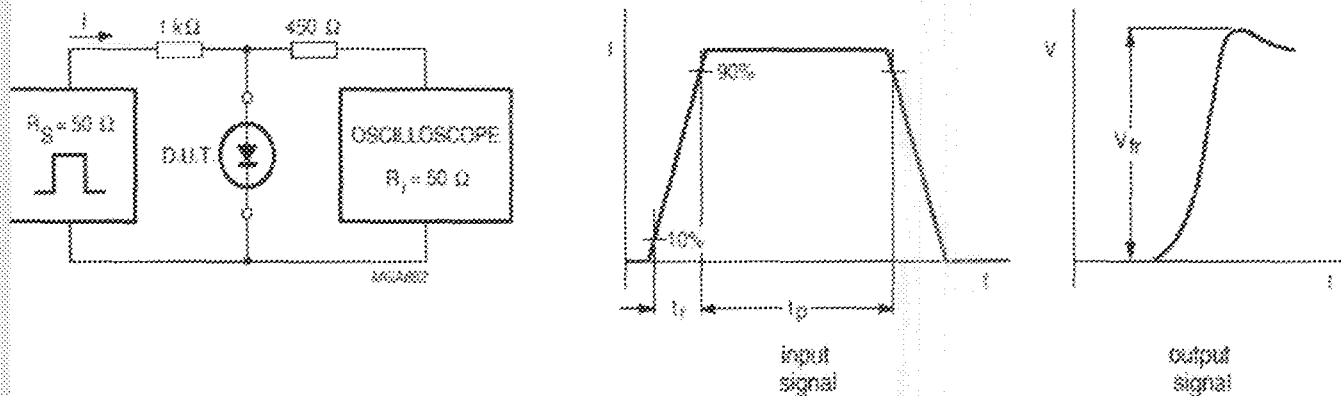
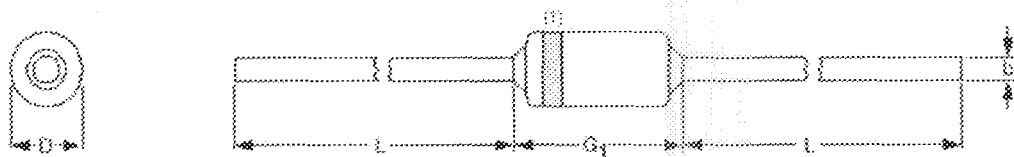


Fig.8 Forward recovery voltage test circuit and waveforms.

PACKAGE OUTLINE

Hermetically sealed glass package; axial leaded; 2 leads



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G_1 max.	L min.
mm	0.56	1.66	4.25	25.4

0 1 2 mm
millimeter
scale

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

GENERAL DESCRIPTION

A N-channel enhancement mode field effect transistor is used in the project they are designed to minimize on-state resistance while providing rugged, reliable and fast switching performance. They can be used in most applications requiring up to 500mA DC. They are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers and other switching applications.
[Transistor BS170]

FEATURES

- High density cell design for low $R_{AS(ON)}$
- Voltage controlled small signal switch
- Rugged and reliable
- High salivation current capability

ABSOLUTE MAXIMUM RATING

$T_A = 25^\circ\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	BS170	UNITS
V_{DS}	Drain Source Voltage	60	V
V_{DGR}	Drain-source voltage ($R_{GS} \leq 1M\Omega$)	60	V
V_{GS}	Gate-Source voltage	± 20	V

I_D	Drain current – continuous	500	mA
	– Pulsed	1200	mA
P_D	Maximum power dissipation	830	mW
	Derate above 25°C	6.6	mW/°C
T_j, T_{STG}	Operating Storage Temperature Range	-55 to 150	°C
T_L	Maximum Lead Temperature For Soldering Purpose, 1/16" from Case for 10 seconds	300	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MINIMUM	TYPE	MAXIMUM	UNITS
<i>OFF CHARACTERISTICS</i>						
BV_{DSS}	Drain-source breakdown voltage	$V_{GS} = 0V,$ $I_D = 100\text{ mA}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 25V,$ $V_{GS} = 0V$			0.5	mA
I_{GSSF}	Gate-body leakage, forward	$V_{GS} = 15V,$ $V_{DS} = 0V$			10	mA
<i>ON CHARACTERISTICS</i>						
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = U_{GS},$ $I_D = 1\text{ mA}$	0.8	2.1	3	V

$R_{DS(ON)}$	Static drain-source on-resistance	$V_{GS} = 10V,$ $I_D = 200mA$		1.2	5	Ω
g_{FS}	Forward transconductance	$V_{DS} = 10V$ $I_D = 200mA$		320		mS

DYNAMIC CHARACTERS

C_{iss}	Input capacitance	$V_{DS} = 10V,$ $V_{GS} = 0V$		24	40	pF
C_{oss}	Output capacitance	$F = 1.0MHz$		17	30	pF
C_{rss}	Reverse transfer capacitance			7	10	pF

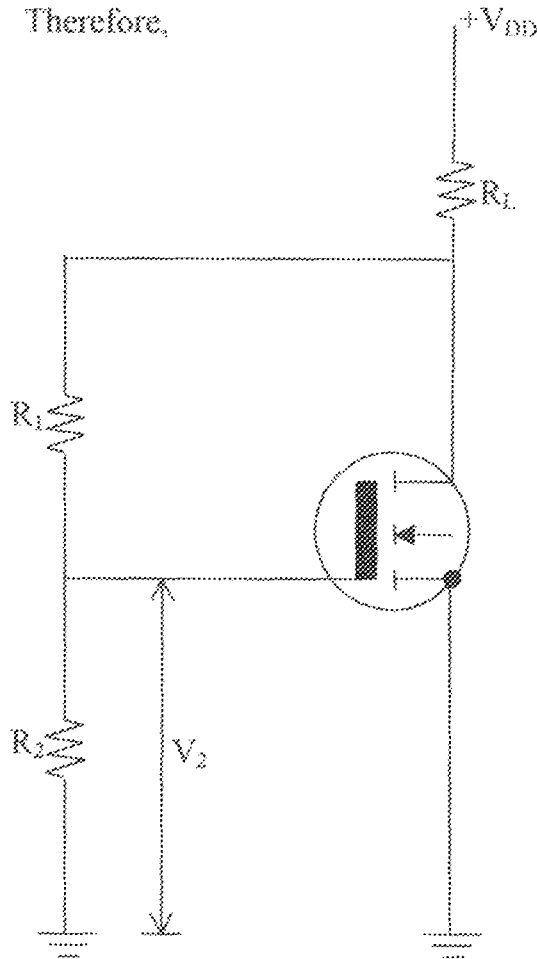
SWITCHING CHARACTERISTICS

t_{on}	Turn-on time	$V_{DD} = 25V,$ $I_D = 200mA$ $V_{GS} = 10V,$ $R_{GEN} = 25\Omega$			10	nS
t_{off}	Turn-off time	$V_{DD} = 25V,$ $I_D = 200mA$ $V_{GS} = 10V,$ $R_{GEN} = 25\Omega$			10	nS

OPERATIONAL CALCULATION

The biasing mode of the transistor as used in the project is the voltage divider biasing mode. V_{DD} going into P_{14} is the required voltage needed to drive the lock circuit from the decoded output of the 4022BC,

Therefore,



$$9 = V_{DD} \frac{220}{220 + 10}$$

$$9 = V_{DD} \frac{22}{23}$$

$$V_{DD} = \frac{9 \times 23}{22}$$

$$V_{DD} = 9.409V$$

Typical Electrical Characteristics

BS170 / MM8F170

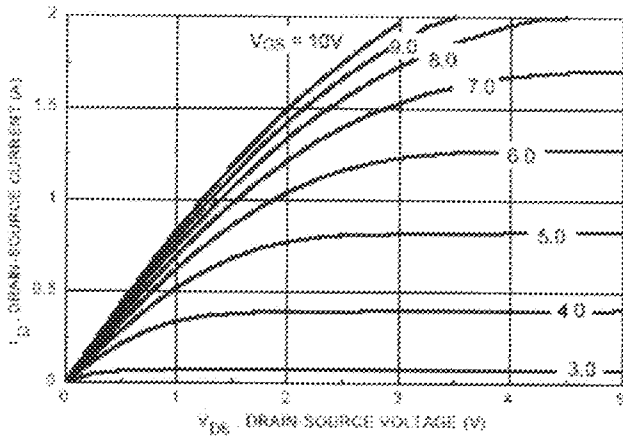


Figure 1. On-Region Characteristics

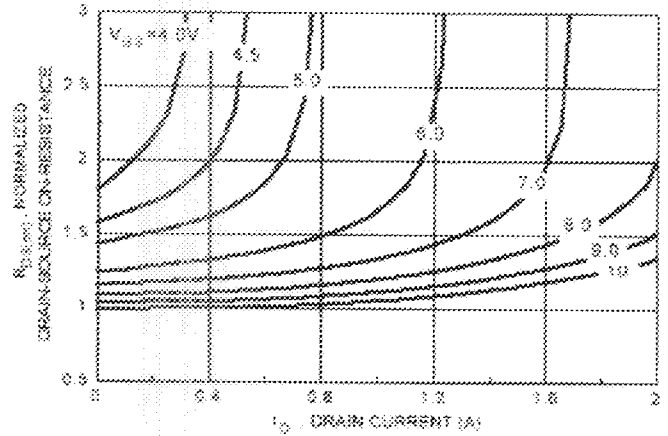


Figure 2. On-Resistance Variation with Gate Voltage

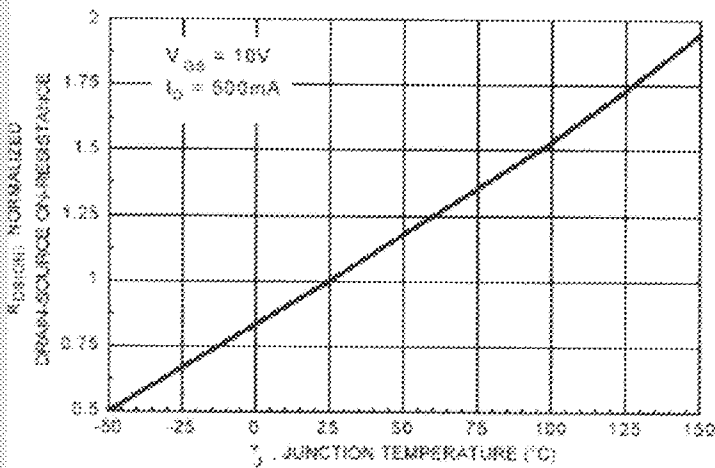


Figure 3. On-Resistance Variation with Temperature

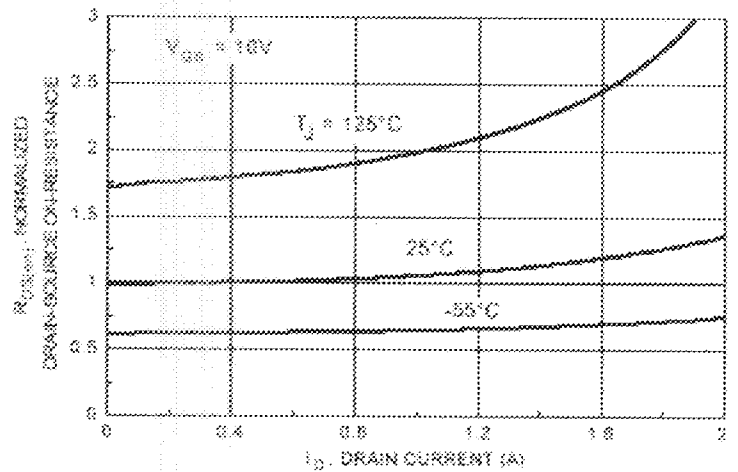


Figure 4. On-Resistance Variation with Drain Current and Temperature

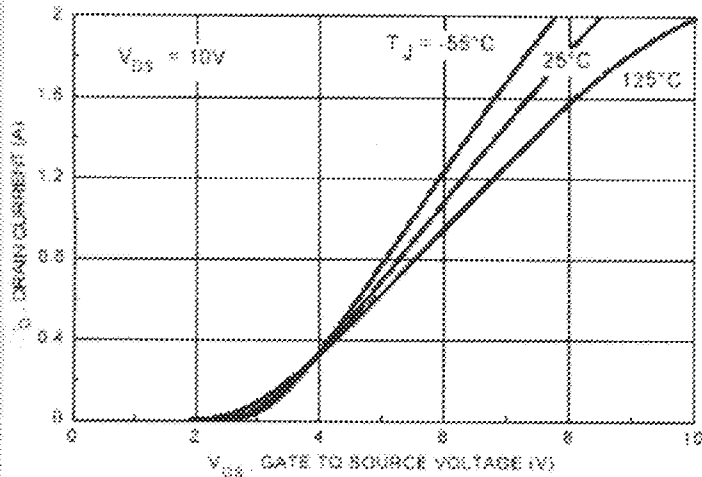


Figure 5. Transfer Characteristics

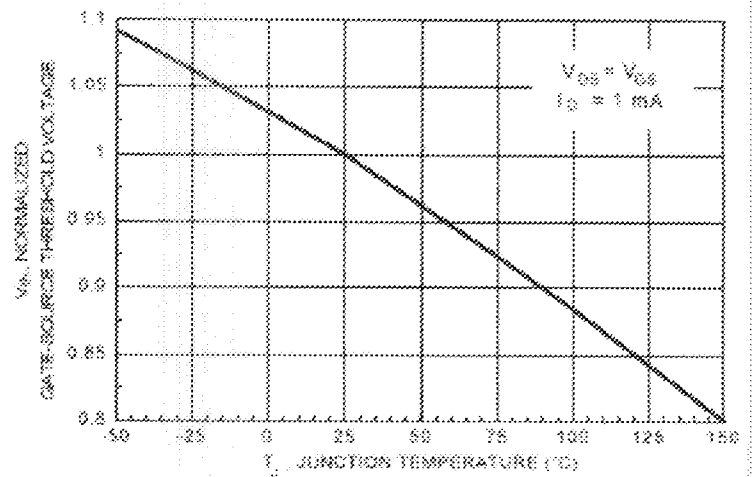


Figure 6. Gate Threshold Variation with Temperature

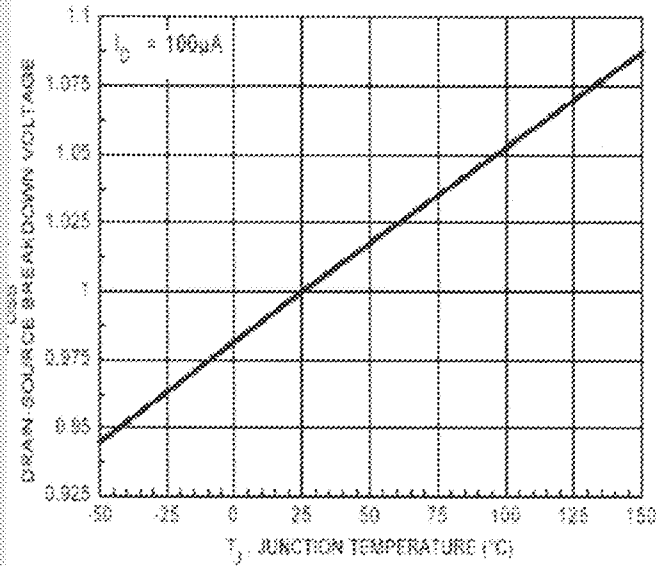


Figure 7. Breakdown Voltage Variation with Temperature.

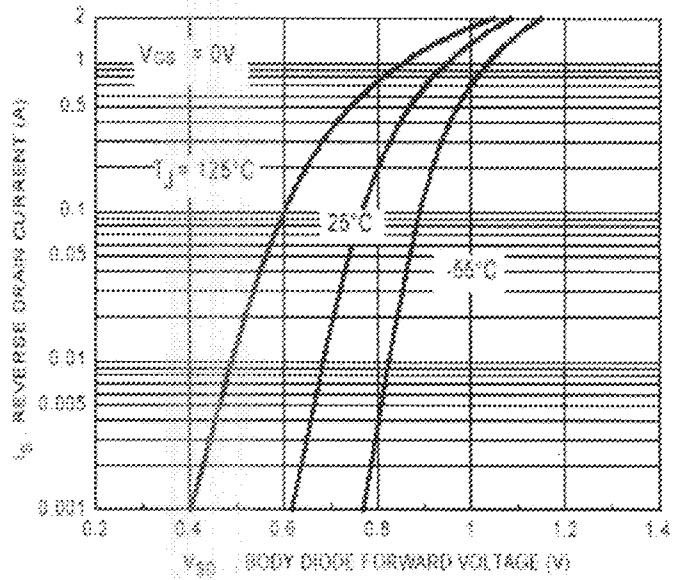


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

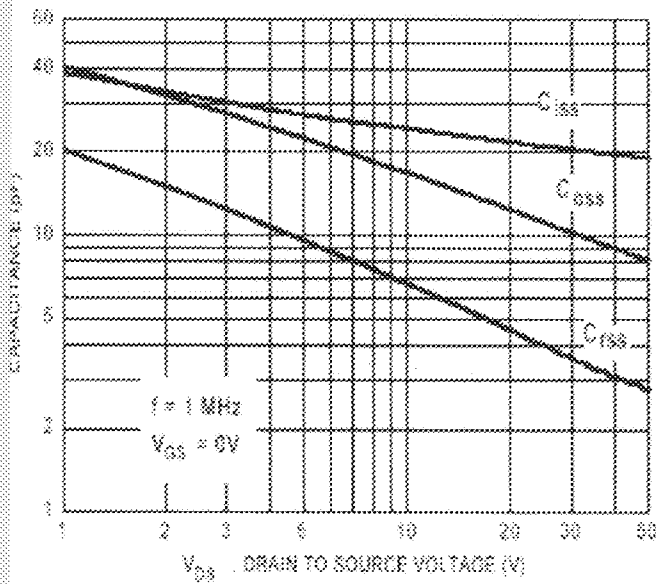


Figure 9. Capacitance Characteristics.

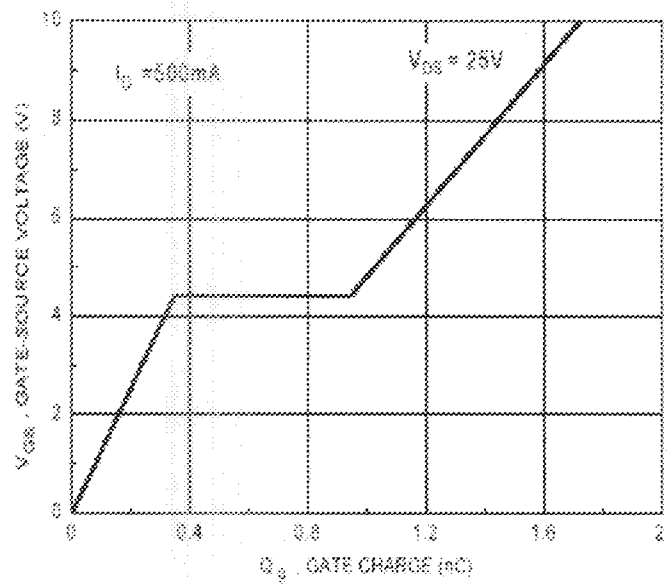


Figure 10. Gate Charge Characteristics.

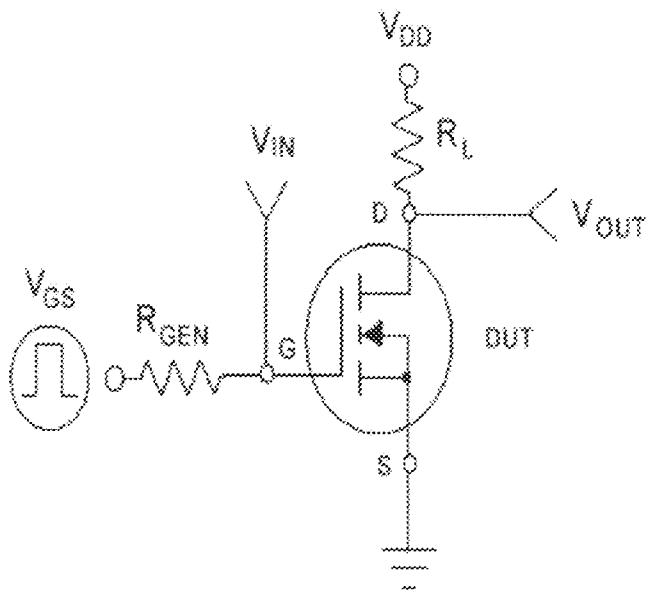


Figure 11. Switching Test Circuit.

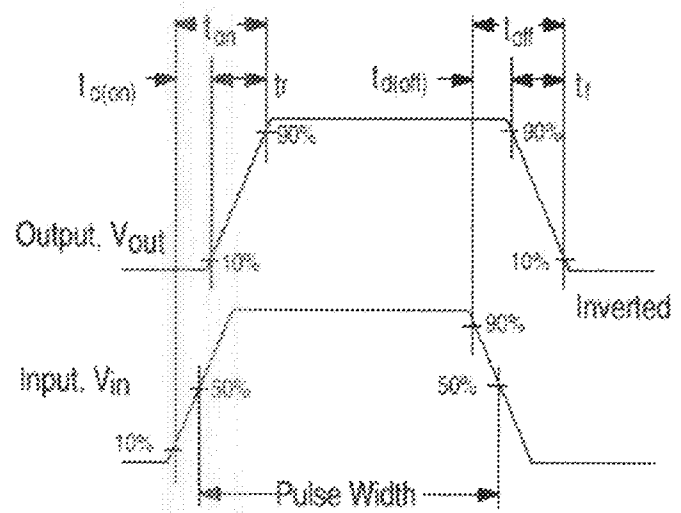


Figure 12. Switching Waveforms.

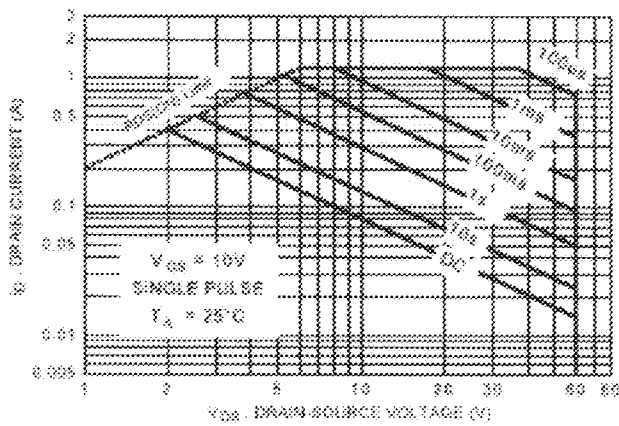


Figure 13. BS170 Maximum Safe Operating Area.

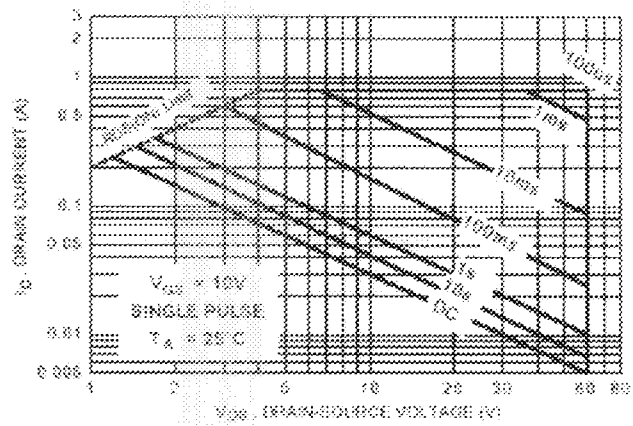


Figure 14. MMBF170 Maximum Safe Operating Area.

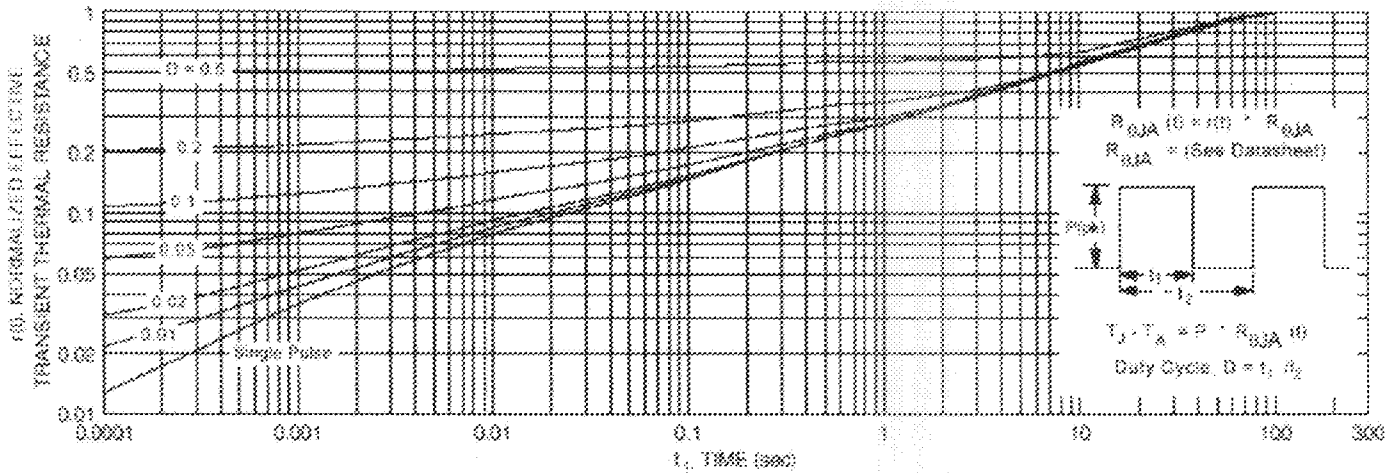


Figure 15. TO-92, BS170 Transient Thermal Response Curve.

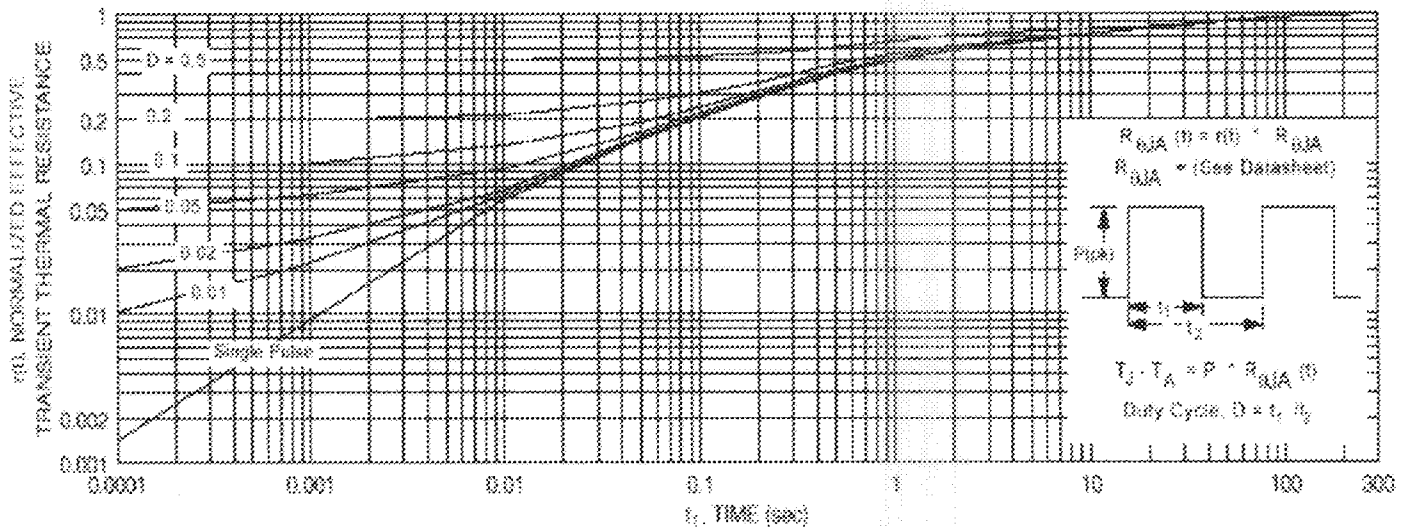


Figure 16. SOT-23, MMBF170 Transient Thermal Response Curve.

INTEGRATED CIRCUIT

Integrated circuit is the most highly sophisticated electron component in use today. It is made up of combination of discrete immature components, such as resistors, capacitors with semiconductor "chips" in which transistor and diodes are fabricated.

There are two groups of integrated circuit, this is often called hybrid integrated circuit. They are constructed by the use of printing circuit board instead of wire to effect inter-connection between the various passive and active component.

The second group of integrated circuit is the monolithic variety because the entire circuit fabrication is done within a single block of silicon crystal. These are common types seen every where. The most common type of integrated circuit package is the dual in-line type, which consist of a plastic bar in which the integrated circuit is embedded. The bar is often almost 20mm long about 5mm wide and barely 2.5mm thick, with the leads protruding out of the two sides.

CD4022BC DIVIDE BY 8 COUNTER/DIVIDER WITH 8 DECODED OUTPUTS

GENERAL DESCRIPTION

The CD4022BC is a four-stage divide by 8 Johnson counter with 8 decoded outputs and a carry-out bit. The counter is cleared to a zero count by a logical "1" on its reset line. The counter is advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at the respective time slot. Each decoded output remains high for one full clock cycle. The carry out signal completes a full cycle for every 10/8 clock input cycles and is used as ripple carry signal to any succeeding stages.

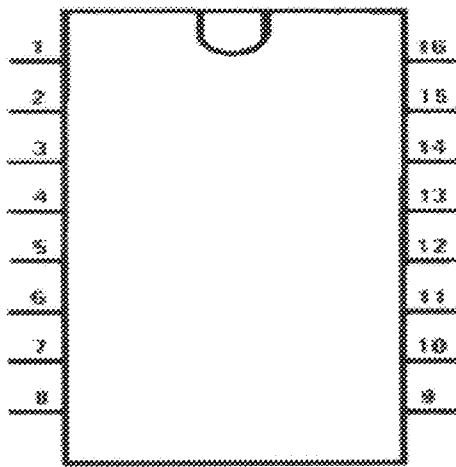
FEATURES

- Wide supply voltage range [3V to 5V]
- High noise immunity [0.45 VDD (type)]
- Low power TTL compatibility [fan out of 2 driving 74L or 1 driving 74LS]
- Medium speed operation [5mHz(type) with 10V V_{DD}]
- Low power [10mW type]
- Fully static operation

APPLICATIONS

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

CONNECTION DIAGRAM



Top View

Order Number CD4022BC Dual – in – line Package

Legend:

- | | |
|------------------------|-------------------------|
| 1 = Decoded output "1" | 9 = NC |
| 2 = Decoded output "0" | 10 = Decoded output "7" |
| 3 = Decoded output "2" | 11 = Decoded output "4" |
| 4 = Decoded output "5" | 12 = Carry out |
| 5 = Decoded output "6" | 13 = Clock enable |

6 = NC	14 = Clock
7 = Decoded output "3"	15 = Reset
8 = V_{SS}	16 = V_{DD}

ABSOLUTE MAXIMUM RATINGS

- DC supply voltage (V_{DD}) $-0.5V_{DC}$ to $+18V_{DC}$
- Input voltage [V_m] $-0.5V_{DC}$ to $+V_{DD} + 0.5V_{DC}$
- Storage temperature [T_s] $-65^{\circ}C$ to $+150^{\circ}C$
- Power dissipation [P_D] Dual in-line 700mW
- Lead temperature [T_L] $260^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

- DC Supply voltage [V_{DD}] $+3V_{DC}$ to $+15V_{DC}$
- Input voltage [V_m] 0 to $V_{DD} - V_{DC}$
- Operating temperature line range $-40^{\circ}C$ to $85^{\circ}C$

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions				Units
			Min	Typ	Max	
I _{DD}	Quiescent Device Current	V _{DD} = 5V, V _{IN} = V _{DD} or V _{SS}		0.5	20	μA
		V _{DD} = 15V, V _{IN} = V _{DD} or V _{SS}		5.0	25	μA
V _{OL}	Low Level Output Voltage	I _O < 1.0 μA V _{DD} = 5V		0	0.05	V
		V _{DD} = 15V		0	0.05	V
V _{OH}	High Level Output Voltage	I _O < 1.0 μA V _{DD} = 5V	4.95	5		V V V
		V _{DD} = 15V	14.95	15		
V _{IL}	Low Level Input Voltage	I _O < 1.0 μA V _{DD} = 5V, V _O = 0.5V or 4.5V			1.5	V
		V _{DD} = 15V, V _O = 1.5V or 13.5V			4.0	V
V _{IH}	High Level Input Voltage	I _O < 1.0 μA V _{DD} = 5V, V _O = 0.5V or 4.5V	3.5			V
		V _{DD} = 15V, V _O = 1.5V or 13.5V	11.0			V
I _{OL}	Low Level Output Current (Note 3)	V _{DD} = 5V, V _O = 0.4V	0.51	0.88		mA
		V _{DD} = 15V, V _O = 1.5V	3.0	8.8		mA
I _{OH}	High Level Output Current (Note 3)	V _{DD} = 5V, V _O = 4.6V	-0.16	-0.36		mA
		V _{DD} = 15V, V _O = 13.5V	-1.2	-3.5		mA
I _{IN}	Input Current	V _{DD} = 15V, V _{IN} = 0V		-10 ⁻⁵	-0.3	μA
		V _{DD} = 15V, V _{IN} = 15V		-10 ⁻⁵	0.3	μA

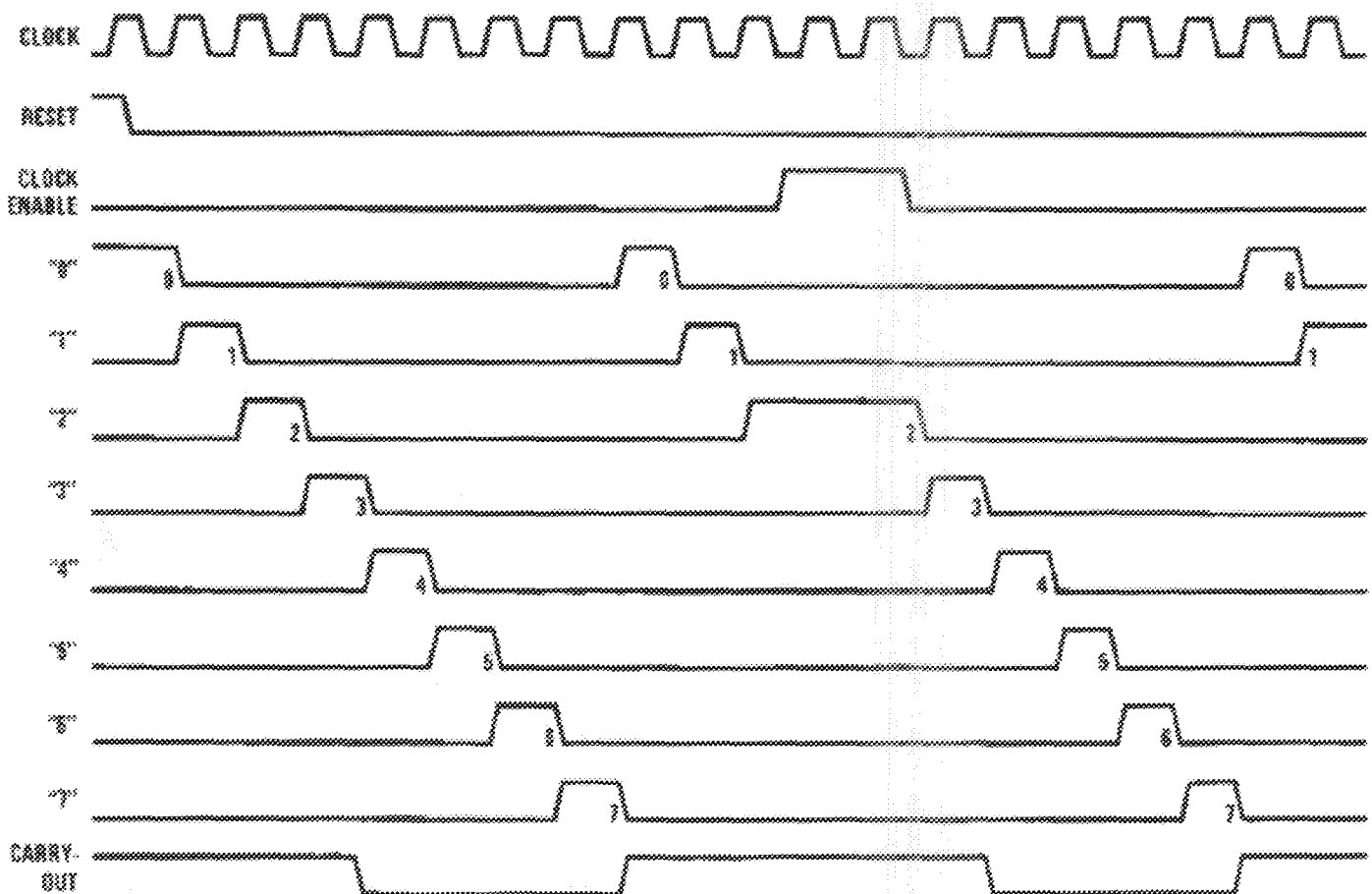
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCK OPERATION						
t_{PHL} , t_{PLH}	Propagation Delay Time Carry Out Line	$V_{DD} = 5V$		415	800	ns
		$V_{DD} = 10V$		160	320	ns
		$V_{DD} = 15V$		130	250	ns
	Carry Out Line	$V_{DD} = 5V$	$C_L = 15\text{ pF}$	240	480	ns
		$V_{DD} = 10V$		85	170	ns
		$V_{DD} = 15V$		70	140	ns
	Decode Out Lines	$V_{DD} = 5V$		500	1000	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{TLH} , t_{THL}	Transition Time Carry Out and Decode Out Lines	$V_{DD} = 5V$		200	360	ns
		$V_{DD} = 10V$		100	180	ns
		$V_{DD} = 15V$		80	130	ns
	t_{THL}	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	Measured with Respect to Carry Output Line	1.0	2	MHz
		$V_{DD} = 10V$		2.5	5	MHz
		$V_{DD} = 15V$		3.0	6	MHz
t_{WL} , t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		125	250	ns
		$V_{DD} = 10V$		45	90	ns
		$V_{DD} = 15V$		35	70	ns
t_{CL} , t_{CD}	Clock Rise and Fall Time	$V_{DD} = 5V$			20	μs
		$V_{DD} = 10V$			15	μs
		$V_{DD} = 15V$			5	μs
t_{SU}	Minimum Clock Inhibit Data Setup Time	$V_{DD} = 5V$		120	240	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		32	65	ns
C_{IN}	Average Input Capacitance			5	7.5	pF

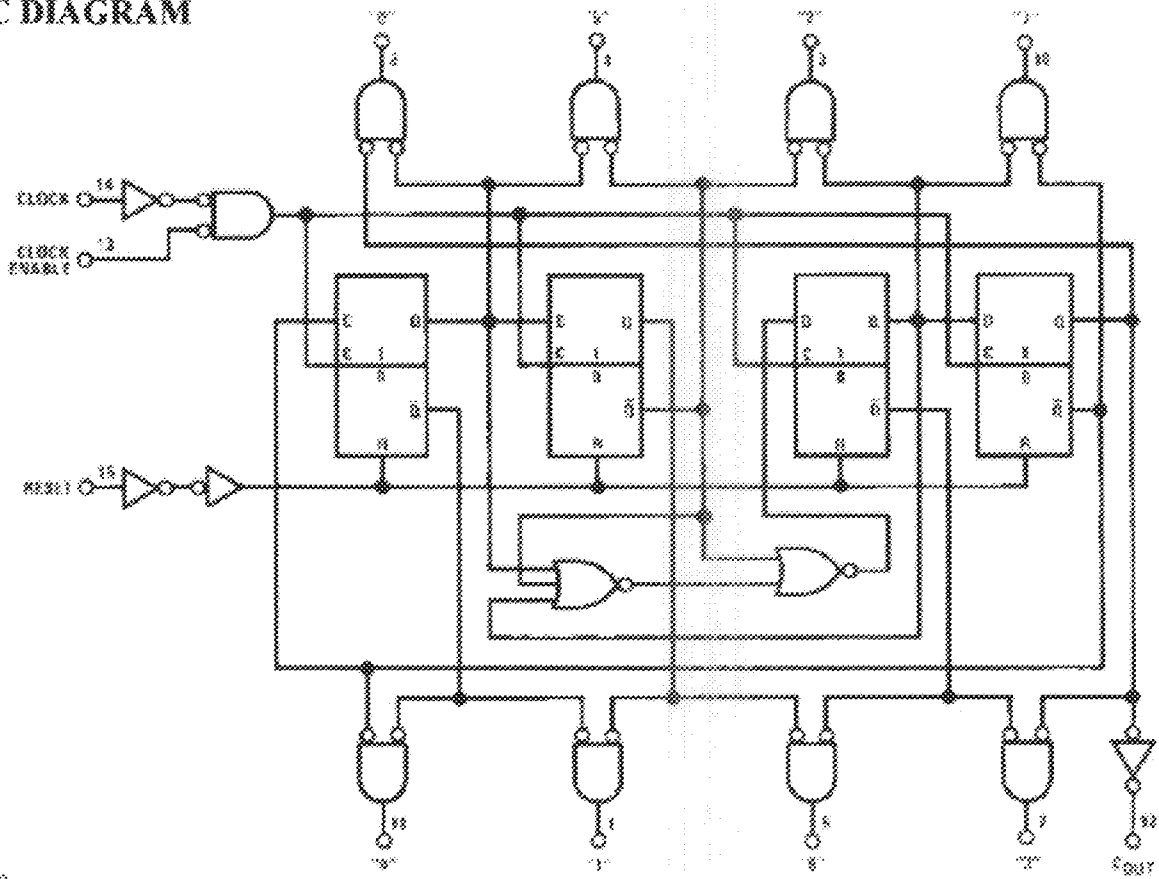
Symbol	Parameter	Conditions	Min	Typ	Max	Units
RESET OPERATION						
t_{PHL} , t_{PLH}	Propagation Delay Time Carry Out Line	$V_{DD} = 5V$		415	800	ns
		$V_{DD} = 10V$		160	320	ns
		$V_{DD} = 15V$		130	250	ns
	Carry Out Line	$V_{DD} = 5V$	$C_L = 15 \text{ pF}$	240	480	ns
		$V_{DD} = 10V$		85	170	ns
		$V_{DD} = 15V$		70	140	ns
	Decode Out Lines	$V_{DD} = 5V$		500	1000	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_w	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		65	110	ns
t_{REM}	Minimum Reset Removal Time	$V_{DD} = 5V$		75	150	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns

$T_A = 25^\circ\text{C}$, $C_L = 50\text{pF}$, $R_2 = 200\text{k}$, $t_{del} = 20\text{ns}$, unless otherwise stated

TIMING DIAGRAM



LOGIC DIAGRAM



Terminal No. 16 - V_{DD}
Terminal No. 8 - GND

TRUTH TABLE OF 4022BC

MR	CP0	CP1	OPERATIONS
1	X	X	00 = 05 - 9 = H; 01 to 09 = L
0	1	/	counter advances
0	.	0	counter advances
0	0	X	No change
0	X	1	No change
0	1	.	No change
0	/	0	No change

- 1: High state (the more positive voltage)
- 0: Low state (the less positive voltage)
- X: State is immaterial
- ∴ Positive --going transition
- /: Negative going transition
- n: Number of clock pulse transition
- MR: Asynchronous master reset input
- CP0: Active low clock input
- CPI: Active high clock input

2.6 SOME GENERAL CONSIDERATIONS DURING THE CHOICE OF COMPONENTS SELECTION

- a) **CD4022B** - Was chosen because the code was intended to be of eight keys, CD4022B has high noise immunity: $0.45V_{DD}$ (type); low power, medium speed and fully static operation.
- b) **BS170** – N – Channel Enhancement Mode Field Effect Transistor was chosen because it is rugged and reliable, it also has high density cell design for low $R_{DS(ON)}$; voltage controlled small signal and high saturation current capacity.
- c) **1N914A High Speed Diode** – was chosen because of its switching speed, continuous reverse voltage, repetition peak reverse voltage and repetitive peak forward current.

CHAPTER THREE

3.0 CONSTRUCTION, TESTING AND RESULTS.

3.1 CONSTRUCTIONS

The construction involves three segments:

1. The door and its frame:- which also serves as the casing for the control unit.
2. The control circuit unit:- which consists the counter.
3. The keyboard:- comprising of the keyboard pad, the 8 number to push – to – on switches.

1. THE DOOR AND ITS FRAME [THE CASING]

In constructing this, the size of the control circuit unit was put into consideration ply wood material was chosen for its light weight ease of modification and it is considerably cheap. A small hole was drilled on the door where the keyboard pad is bolted over.

2. THE CONTROL CIRCUIT

Following the control circuit design, the component layout was first sited. The components to be connected on the circuit board were first handled. Taking good note of component spacing, clearance, direction and proximity; solid connection soldered joints were made and its positions were then placed

appropriately. All other components were positioned with respect to the system circuit diagram.

Copper (cord) strips that are unused are scrapped off at the point where components terminate to ensure that short circuit is avoided. These careful and professional precautive steps were followed until all the components were assembled according to the design.

3. THE KEYBOARD

The keyboard pad was made from an office calculator button pad. The switches were carefully placed in the calculator buttonholes and the number codes are gummed onto the switches with adhesive. A small hole was drilled with a small bit-drilling machine to allow access to the switches through the keyboard that was bolted to the doorframe.

3.2 TESTING

The system was tested as follows after the construction:

1. When unconnected to power supply mains;
2. When connected to power supply and wrong code entered;
3. When connected to power supply and right code entered.

3.3 RESULTS

1. When the system was unconnected to the power supply mains, the door remains locked.

2. When connected to the power supply main and wrong code were entered, the door remained locked.
3. When connected to power supply mains and right code entered, the door was unlocked.

3.4 DISCUSSION OF RESULTS

From stated results, it implies that it is unlocked when the correct code is entered.

CHAPTER FOUR

4.0 CONCLUSION AND RECOMMENDATIONS

4.1 CONCLUSION

Going by the scope of this project work, the set objectives of the design as desired such as the systems accessibility, user friendliness, reliability and most importantly, security have been virtually achieved.

4.2 RECOMMENDATIONS

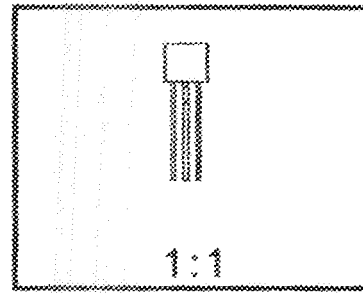
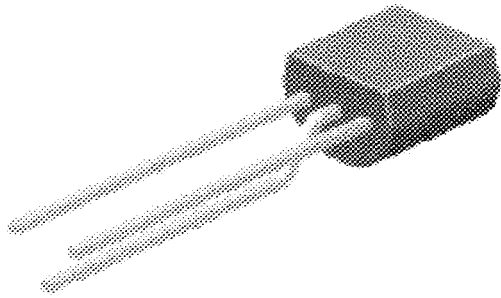
For domestic and office installation and actualization of this project, another by pass switch could be made and positioned in another safe room in case of the system failure

REFERENCES

Text Book of Electrical Technology, By B. L. Theraja & A. K. Theraja

www.National.com

APPENDIX A: MANUFACTURER DATA SHEET FOR BS170



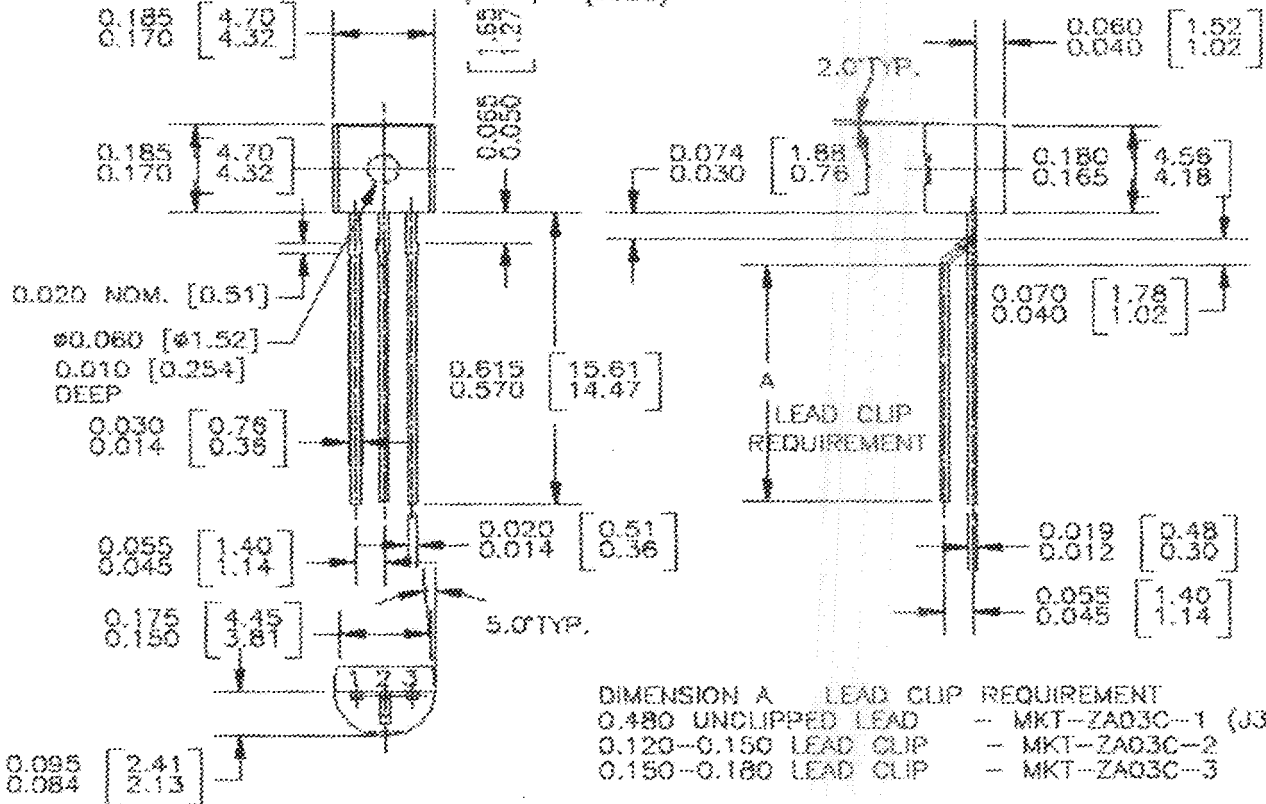
1:1

Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

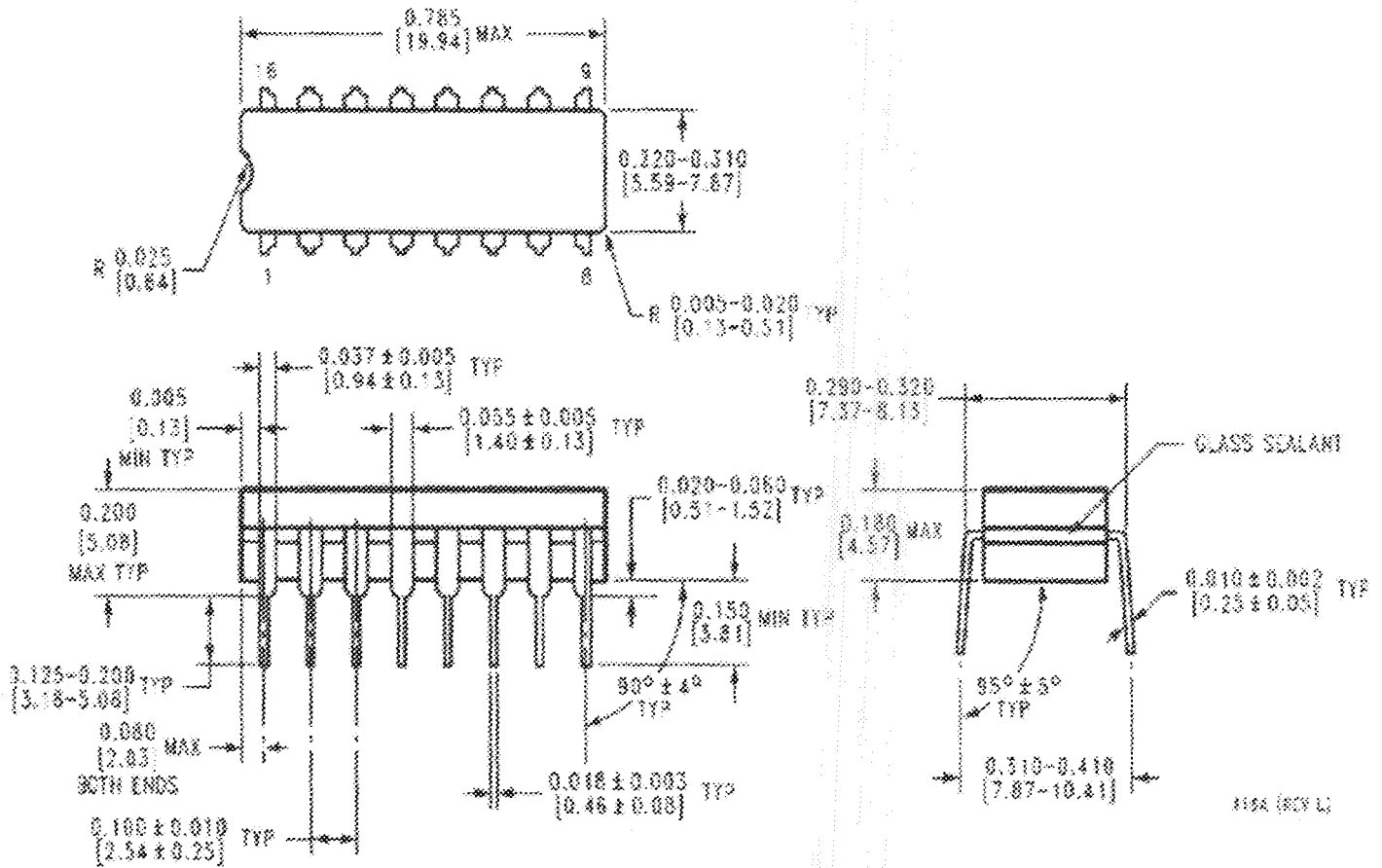
Part Weight per unit (gram): 0.22

TO-92(92,94,96,97,98*)
TO-18 REVERSE LEADFORM
(J35Z)



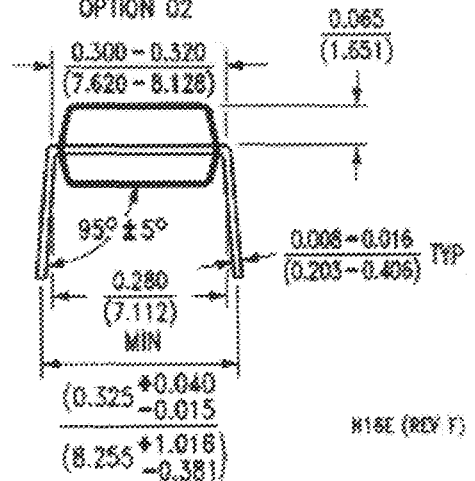
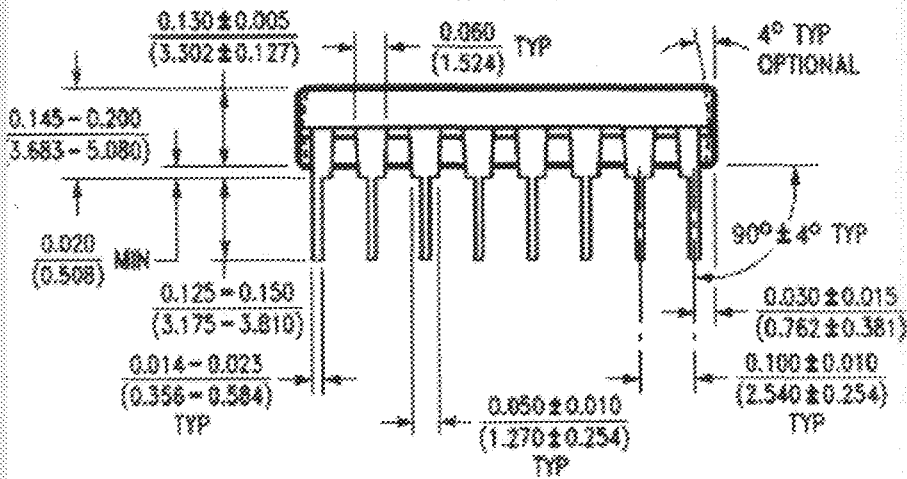
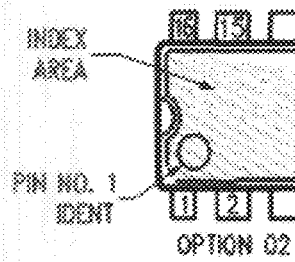
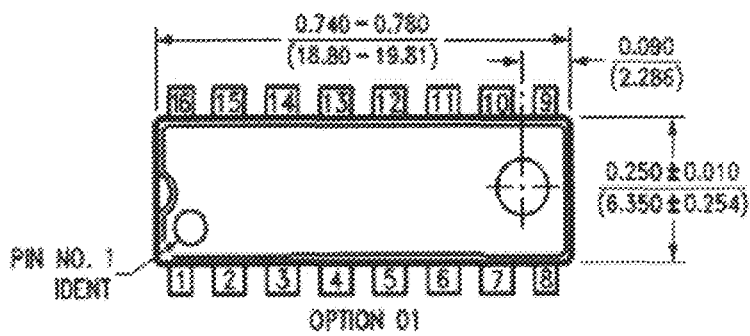
APPENDIX B : MANUFACTURER DATA SHEET FOR CD4022B

Physical Dimensions inches (millimeters)



4164 (REV L)

Ceramic Dual-In-Line Package (J)
Order Number CD4017BMJ, CD4017BCJ, CD4022BMJ, CD4022BCJ



H16E (REV F)

Molded Dual-In-Line Package (N)

Order Number CD4017BMN, CD4017BCN, CD4022BMN, CD4022BCN