DESIGN AND CONSTRUCTION OF DIGITAL DIMMER SWITCH WITH DISPLAY UNIT.

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THIS PROJECT IS SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING IN PARTIAL FULFILMENT OF THE REQUIREMENT FOR THE AWARD OF BACHELOR OF ENGINEERING (B.ENG). DEGREE.

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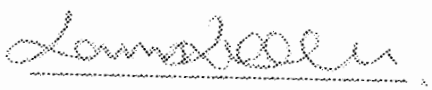
DECLARATION.

This is to declare that I SANNI KASSIM OLAKUNLE of Electrical and Computer Engineering Department of Federal University of Technology, Minna carry out this project, under the supervision of **Engineer Asula . T**



Signature Of Student

CERTIFICATION

This is to certify that this project was carried out by ***SANNI KASSIM OLAKUNLE*** of Electrical and Computer Engineering Department of Federal University of Technology, Minna, under the supervision of **Engineer .T. Asula**

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.....

EXTERNAL EXAMINER

Date: .....

DEDICATION

I dedicate this work to Almighty Allah for His loving kindness, guidiance, and protection and to my late father Mr. ***A. O. SANNI.***

ACKNOWLEDGEMENT

The completion of this project calls for the acknowledgement of those who contributed immensely to the success of this work.

First and foremost, my thanks goes to almighty Allah for His protection, provision and guidance through out all of my stay in the university. I acknowledge the contribution of the Head of Department.

My unreserved and sincere gratitude goes to my Supervisor Engr. Asula. May God bless you all Sir.

My unreserved gratefulness goes to my mother Alhaja M.A SANNI and her brother Engr W.A Momoh for their support, encouragement, love and care through out the period of my academic carrier.

I must not forget to express my profound gratitude to my brothers and sisters, Dapo, Tunde, Demola, Jide, Bola, and Olaide. They have been a source of blessing. I must acknowledge my gratitude to my friends, Abdulazeez Muslimat, and Princess Kehinde Olaonipekun, for their encouragement and support, may the countenance of almighty Allah ever shine on them.

My profound gratitude goes to Mrs Dapo - Sanni and their children, may Almighty Allah rain His showers of blessing on you and the entire family.

ABSTRACT

Design and construction of dimmer switch with digital display unit is described in this report.

The project is design to dim an electric current. There are basic stages in this project, these are dimmer switch, display unit and control unit system, which consist of a triac, diac circuit used to give sample on/off type of power control. And the display unit output.

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CHAPTER ONE

1.0 GENERAL INTRODUCTION.

1.1 INTRODUCTION

Light is everything in our home. The light level in a room affects the way we do our day-to-day activities, and it has huge effect on how we feel. It is difficult for us to read under a single candle, and a romantic for two isn't so romantic under a 1,500-watt halogen Lamp.

The issue is that we need to use some room for many different purpose and different functions calls for varying amount of light. This is when the Light dimmer switch comes into places: a handy electrical component that let's you adjust light levels from nearly dark to full lit by pressing soft-touch button.

An effective way to quickly change the mood of a room is by dimming or brightening the light with a dimmer switch. A softer light results in a more comforting, relaxing atmosphere. Brighter lighter is more suitable for normal room use and reading. Any easy way to control your lighting is to install a dimmer switch.

1.2 Aims and Objectives

The aims of this project is to design and construct a dimmer switch with digital display. It works as a high speed power switch which works at a potential up to several hundred volts and can handle current up ten or hundred of amps.

It is intented that this project will be able to regulate the light intensity of a lamp or the speed of electric motors by regulating the voltage.

Some current application of Dimmer Switch System are:-

Household application: - Dimmer switches are used in our homes to dim electric lamp intensity and they are also used in electric cooker, electric fan.

Industrial application: - Used in regulating the speed of an electric motors.

1.3 Theory of the Operations

This project contains three major building blocks each of which was designed, using discrete component as well as IOS. These blocks are light dimmer, control unit and display circuit.

The dimmer circuit is built around a uni-junction transistor which forms a basic oscillator and generates pulse, which are generated by a capacitor placed at it's gates in a voltage – divider connection with a

resistor switches.

The pulse generated by the uni-junction transistor are applied to the gate of a triac which is turn, is used to switch on the main load which is the bulb. A 250k

variable resistor is used to vary the phase which these pulses are applied from 30^{0} to 120^{0} hence the circuit dimmer action.

The last block is display circuit connected in parallel with the to sense the output.

1.4 Literature Review

Light dimming is based on adjusting the voltage to the lamp to emit small amount of light. Light has been possible for many decades by using adjustable power resistor and adjustable transformers. Electric controlling also made it possible to make them easy controllable from location.

Some years back, this was usually done by using rheostat, a large variable resistor. This generated huge amount of heat and wasted electricity. To control the amount of energy going to the light, the rheostat had to ignore some electricity and turn it to heat. For example, at half brightness a 100watt bulb would waste about 20watt to heat in the rheostat.

Modern dimmer takes a more efficient approach instead of directing energy from the light bulb to the rheostat. Modern resistor rapidly shut the light circuit off and on to reduce the total amount of energy flowing through the circuit.

Modern light dimmer takes switches use a transistor- life device called a Triac and diac to trigger the electricity on and off very rapidly because the sort of 'chop up' the electrical power this way they are sometimes called 'Chop Switches'. The current does not change suddenly.

1.5 Project Outlines

This project is divided into four chapters. Chapter one discusses general introduction of the project, some current application of dimmer switch systems, the aims and objectives of the project, the construction and analysis of the project and literature review.

Chapter two is on system designs. Here is calculation leading to choice of component used are shown. Chapter three is design with construction, testing and results.

The method of construction and the construction boxes containing the circuit discussed here.

Chapter four is for conclusion and recommendations.

CHAPTER TWO

2.0 SYSTEM DESIGN

2.1 THE POWER OF SUPPLY UNIT.

The A/D converter used in this project design required a dual voltage supply of 15V. The connection of the power unit is shown in Figure 2.1. The circuitry consist of 12V center tap transfer whose output are fed into the diode bridge rectifier to produce a d.c voltage output some capacitors of specified capacitance values were used to remove ripples by way of filtering. The 7805 and 7905 IC voltage regulators were used to produce constant d.c voltage supply +5V and –5V respectively which is required to power OP amp IC chips used in the used in the project and to drive ICL7107. No converter, while pin 21 is grounded.

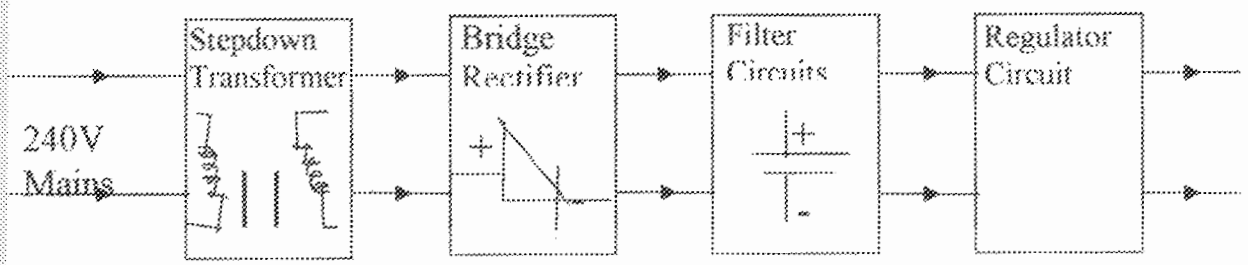
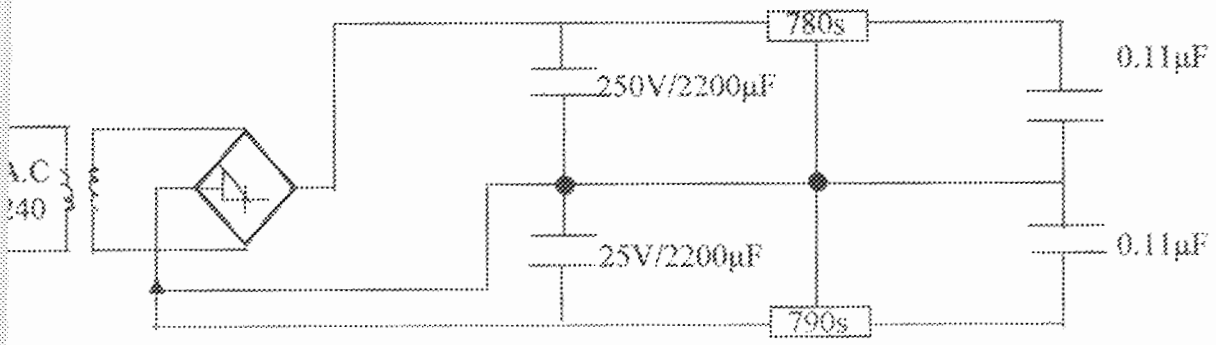


FIG. 1 Block Diagram of Power Supply



DUAL VOLTAGE & POWER SUPPLY UNIT

2.1.1

i TRANSFORMER SELECTION

P_o = Vdc X Idc

= 2Vm / π X 2Im/ π

= $2\sqrt{2}$Vrms / π X $2\sqrt{2}$Vrms/ π X Vrms/R

= 8 Vrm^2s/π^2R

Therefore

Vrms = $\sqrt{P_o\pi^2R/8}$

For this project

P_o is 6□, R_2 = 9Ω

Vrms $= \sqrt{6 \times \lambda^2} \times 9/8$

$= 6.9914V$

$= 6V$

ii **DIODES RATING**

Voltage rating: - the maximum voltage, which occurs across the diode in the reverse direction peak inverse (PIV) must be less than the break down voltage of diode if it not conduct appreciably in the reverse direction.

Foe a full-wave

PIV $= 2Vm$

Vm $= \sqrt{}2Vrm$

$= \sqrt{2} \times 12$

$= 16.197V$

Vm $= 17V$

Therefore

PIV $= 2 \times 17 = 34$ V

iii. **Capacitor Selection**

Voltage rating

Capacitor Voltage Vc rating $\square \sqrt{2}$ Vrms

$\sqrt{2}$ X 12 = 16.97V ($\sqrt{2}$Vrms)

Vc □ $\sqrt{2}$ Vrms

Vc □ 16.97V

Therefore a capacitor of voltage rating of 25V was chosen.

Capacitance rating

$\triangle V = Vm/ 2FRC$

$\triangle V \square //C$

If a Peak – to – peak ripple voltage of not more than 10V is to be tolerated

$10 = 12\sqrt{2}/(50 \times 8 \times C)$

$C = 12\sqrt{2}/8000$

$= 212\mu F$

Therefore a capacitor of 2200μF capacitance was chosen.

2.1.2 The Rectifier (Bridge) W01

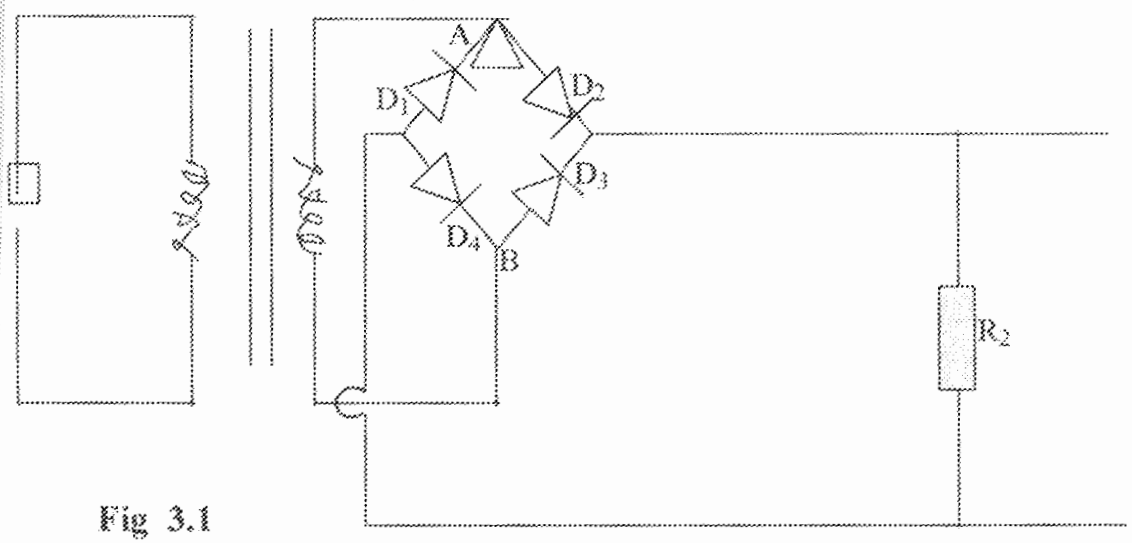


Fig 3.1

A rectifier is the arrangement of diodes to convert AC Voltage a pulsating DC Voltage. For analysis, we shall limit our scope to full-ware bridge type of rectifier. The full ware bridge use four diodes arranged in bridge shown as in Fig. 3.1

During the half cycle of the input at point A positive w.r.t. B diodes D_2 and D_4 blocks current flow from B to A through D_3 R_2 and D_1 both current passes through the load, R_2 in the same direction and so a fluctuating un-directional voltage is developed across the load having the wave as shown in Fig. 3.2

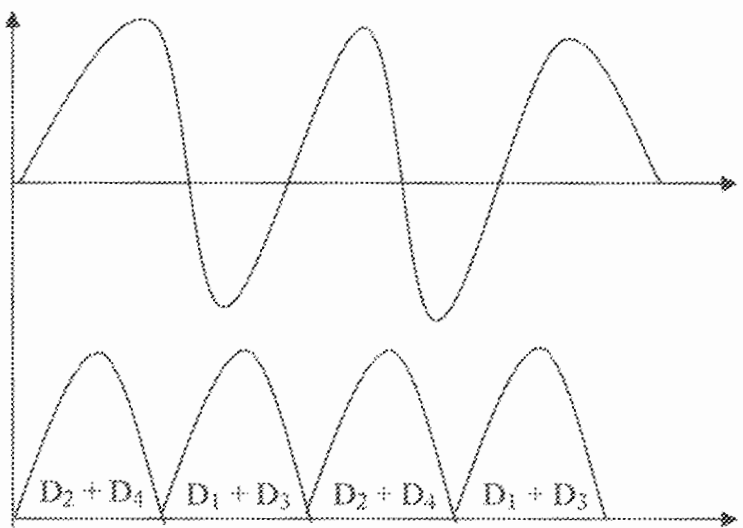


Figure 3.2

In considering rectifier for design purposes it is always important to know the peak voltage, PIV that appears across the diodes. The PIV of a full wave bridge type is twice the maximum voltage.

2.1.3 A.C FILTERING / SMOOTHENING

A half or full wave rectified- voltage wave form smoothened out to provide an approximate d.c. voltage using a capacitor shunted across the load to act as a filter. The capacitor stores energy during the conduction period and delivers this energy to the load during the non-conducting period. The deviation of the load voltage from it average or d.c. value is referred to as the ripple voltage.

Referring to the Fig.4.1 which show the half-wave rectifier circuit with capacitor smoothing and the associated output voltage and diode current wave forms,

The following simplifying approximation are:

(a) The source of impedance is negligible

(b) The forward voltage across a conducting diode is assumed constant irrespective of currents

(c) The diode current is assumed to be triangular

(d) The diode switching time □ when the capacitor is fully charged occurs at the peak of the supply voltage (i.e. □ wt = /2)

(e) The load time constant (R_L is large compare with the period of the rectifier output wave form, so that the charging interval □C is small compared the cycle time T.

Considering the waveform, for half-wave rectifier show in fig a.

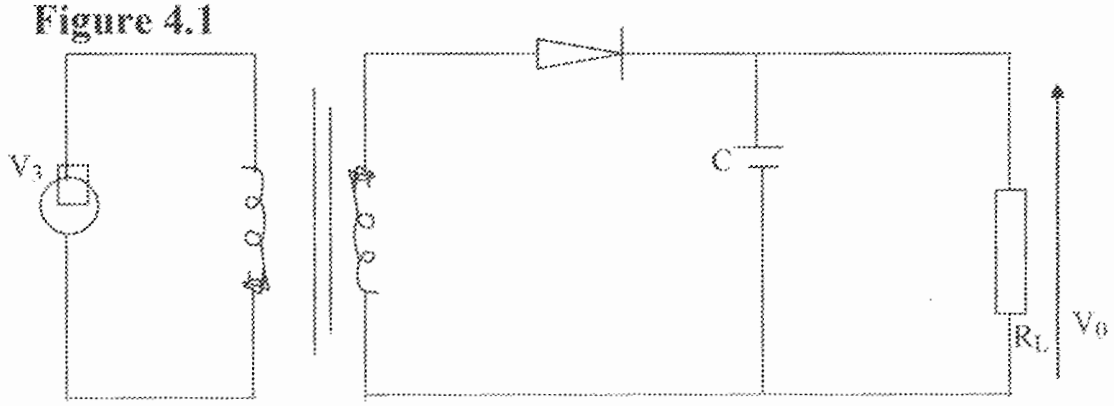
$$V_{dc} \approx V_m - V_r/2$$

and

$$\sin \theta_1 = \frac{V_m - V_r}{V}$$

$$= \sin^{-1}\left\{\frac{V_m - V_r}{V_m}\right\}$$

Figure 4.1



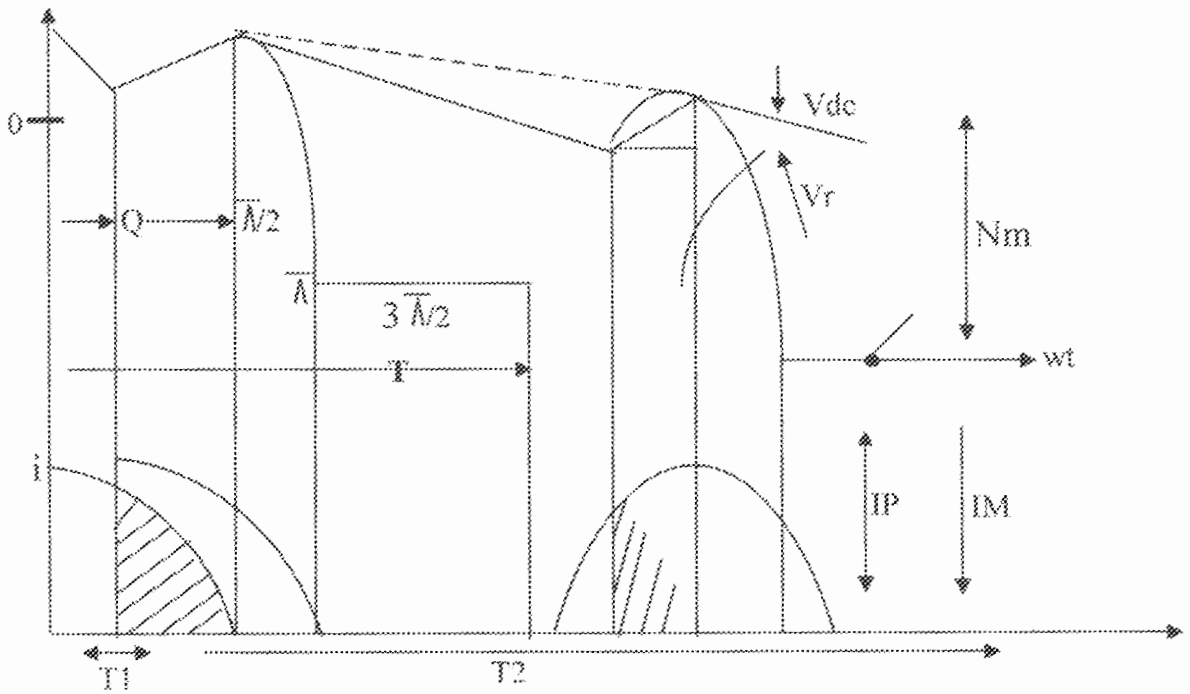


Fig 4.2 Half wave rectifier with capacitor Smooth

2.1.4 Amplification

The second stage is the collector base baise amplifier, which amplifies the input voltage i.e the voltage across the infrared. This is coupled via the capacitor CI. The transistor used is Bc/09 with Life 2520. The first stage has a voltage given of 7.5V. Thus is further amplifier by the second stage which has a voltage given of 6.5V, this is to improve the stability of the output.

2.1.5 Switching

Sine wave is the output from the amplifier, pulses of Q^3 to be positive the input to be inverted and pulse generated hence diode D_2 & D_3.

During the positive half circle diode D_3 conduct to be ground while negative half circle diode D_2 will conduct (half - wave rectification).

But $\square_2 = \frac{1}{\lambda}$

$$0c = \square_2 - \square_1 = \frac{1}{2} - \text{Sin}^{-1}\left[\frac{Vm - Vr}{Vm}\right]$$

$$\text{or Cos}\theta\ c = \left[\frac{Vm - Vr}{Vm}\right]$$

During the charging period, the accumulated in the capacitor C is given by Q = CV.

This charge is mostly transferred to the load during discharge, the charge lost by the

Q = Idct,

Since $T_{\frac{1}{2}} = T$

$$IdcT = Cvr$$

$$Vr = \left[\frac{IdcT}{C}\right]$$

But $T = \left[\frac{1}{fc}\right]$

$$Vr = \left[\frac{Ldc}{Fc}\right]$$

And $Vdc = IdcR_{L} = fcR_{L}Vr$

The ripple factor Y is given by

$$r = \frac{\text{r.m.s value of all a.c components}}{\text{d.c. components}}$$

Since we have assumed that the ripple has a triangular wave form of peak value

Vr/2 its r.m.s value can be shown to be

$$\frac{Vr \times 1}{2 \quad \sqrt{3}}$$

$$r = Vr \ / 2\sqrt{3Vdc}$$

For the full-wave coase, the wave form period is that for half-wave.

$$\therefore T_{\frac{1}{2}} = 1/2f$$

$$Vr = \frac{Idc}{2fc}$$

2.1.6 S.C.R.S

S.C.R.S and trials are members of the thyristor family. They act as high-speed power switches. They are soled – states devices and can operate at potentials up to several hundred volts and can handle current up to tens or hundred of amps. They can be used to replace conventional mechanical switches and relays in many d.c. and a.c. power control systems and can readily be used to control electric lamps, motors, heaters and alarms.

The S.C.R or silicon controlled Rectifier, is a four-layer pnpn silicon semiconductor device and is represented by the symbol shown in figure 5.
Note that this symbol resembles that of a normal rectifier, but has an additional terminal known as the gate. The S.C.R can be made to act as either an open-circuit switch or as a silicon rectifier, depending on how its gate is used.

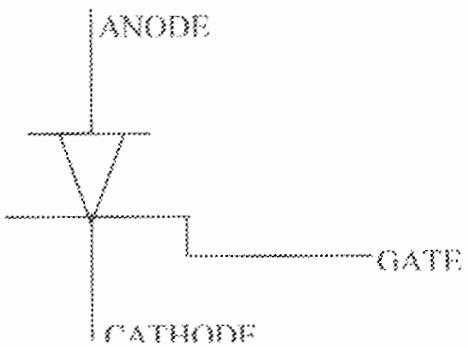


Fig 5

2.1.7 ZERO – CROSSING DETECTOR

The circuit shown in fig 5 generates an output square wave for use with TT_2 Logic (zero to – to 5v range) from an input wave of any amplitude up to 100volts Rv combine with D_1 and D_2 limits the input swing to – 0.6 volt to +5volts, approximately. Resistive divider R2R3 comparator. R3 and R6 provide hystereses with R4 setting the trigger points symmetrically about ground. The input impedance is nearly constant, because of the large R1 value relative to other resistor in the input attenuator. A 393 is used because its inputs can go all the way to ground making single supply operation simple.

2.1.8 PHASE TRIGGERING CIRCUIT

Figure 6 shows the basic phase – trigged circuit using a trial as the power control element. The load is wired in series with the trial and the combination is connected across the a.c power line. The trial gate – trigger – device. The phase – delay net – work enabled a.c. voltage to the input of the trigger device to be delayed to that on MT_2 by an amount fully variable from (ideally) 0^0 to 180^0 i.e by as one half – cycle line voltage.

The trigger device is voltage – operated switch that triggers on and fires the trial when a preset voltage is reached at output of the phase delay network or at the end of the preset phase delay period.

Figure 6.1 shows the wave – form that occurs in different sittings of phase delay network is set only a 10^0 delay the trial is trigged on 10^0 after the start of each half-cycle. And then self –latches and stays on the remaining 170^0

of each half – cycle. Almost the full available line power is thus applied to the load under this condition.

If the circuit is set for a phase delay of 90^0, the trial does not turn on until half –way through each half – cycle and only half of the maximums possible power is applied to the load under this condition. Thus, the load power can be varied the setting of phase – delay control since the trial is either fully off or is saturated at all times very little power is 'lost' in device and very efficient available power control is obtained.

The actual phase – delay section of fig. 1.1 circuit can take either of two basic forms. It can consist of either a single or multiple R – C variable phase shift network or an R – C variable time – delay network.

2.1.9 DISPLAY CIRCUIT ATTENUATION

This connected in the 2v display made. The precision rectifier is fed with 1v and the output varied through a variable resistor between 0 and 2v. The 300Vac from the dimmer circuit must be attenuated; this is done through voltage divider network at a ration of 300V:1V for the mains voltage to precision amplifier input respectively. The figure 6 shows below; the voltage divider network.

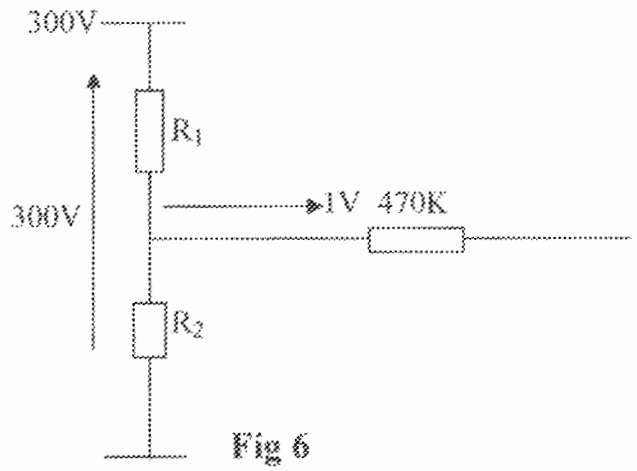


Fig 6

Current across R_1 &R_2 is the same

where $V_1 = V$

A1 = 15mΩ

Using voltage divider

$$V1 = \frac{R_2 \times 300}{R_1 + R_2}$$

$$L = \frac{R_2 \times 300}{15 \times 10^6 + R_2}$$

$15 \times 10^6 \times R_2 = 300R_2$

$15 \times 10^6 = 299R_2$

$$R_2 = \frac{15 \times 10^6}{299} = 50K\Omega$$

$R_2 = 50K\Omega$

2.2.0 PRECISION AMPLIFIER

The precision amplifier is of two these are:

(a) The precision half wave rectifier

(b) The precision full wave rectifier

For the purpose of this project full wave rectifier was used.

b) The Precision full wave rectifier

The half – wave circuit can be adapted in various ways to provide precision full wave rectification. A common form is shown in Fig 6. Amplifier A provides half – wave rectification blocking the negative half – cycles of the input and inverting the positive half – cycles with a gains of unity. Amplifier a_2 is a summing inverting amplifier with a given –1 for input signal v1 and against of –2 for the rectified output V_{01}. The waveforms are shown in figure 7 waveforms (c) and (d) show the output of A_2 resulting from the two inputs taken separately. Output(c) is the sum of the other two precision rectification requires tight tolerance resistor for R_1R_2 and R_5. If an average of d.c output required, the IμF capacitor shown can be added to the circuit converting A_2 into a summing integrator.

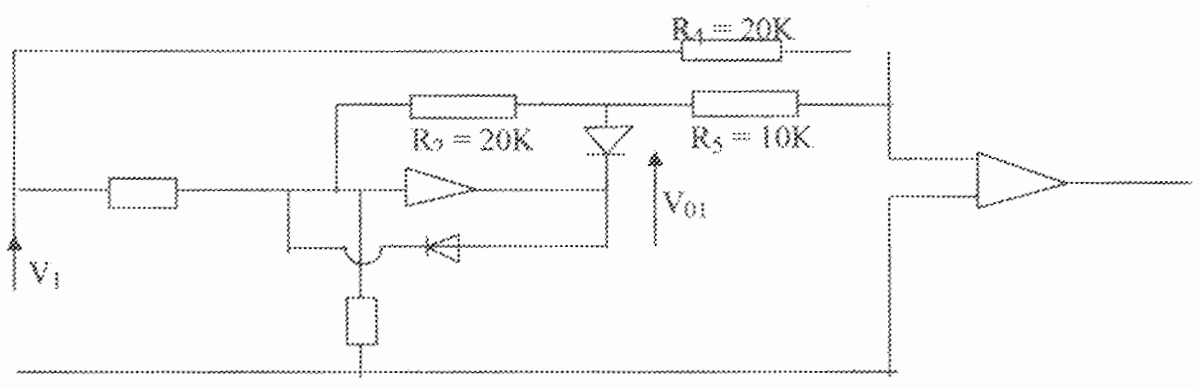


Fig 7 THE PRECISION FULL WAVE RECTIFIER

2.2.1 INFRA RAY EMITTING DIODE

The **HCC4017B** (extended temperature range) and **HCF4017B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and plastic micro package. The **HCC/HCF4017B** and **HCC/HCF4022B** are 5-stage and 4-stage counters having 10 and 8 decoded outputs, respectively.

Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times. These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the decade-counter configuration permits high-speed operation, 2-input decimal-decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence.

The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the **HCC/HCF4017B** or every 8 clock input cycles in the **HCC/HCF4022B** and is used to ripple-clock the succeeding device in a multi-device counting chain.

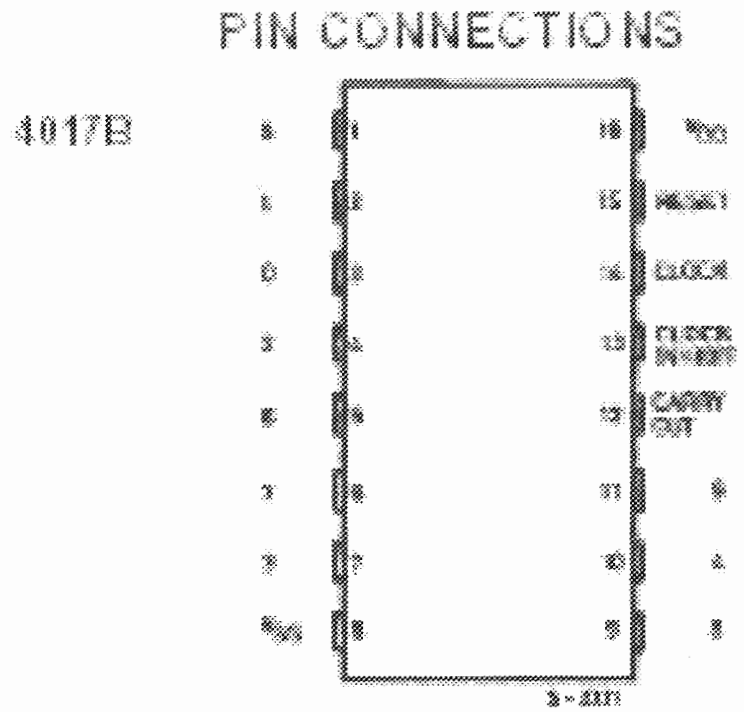


FIG.8 Pin Connections for the Infra ray emitting diode (4017B)

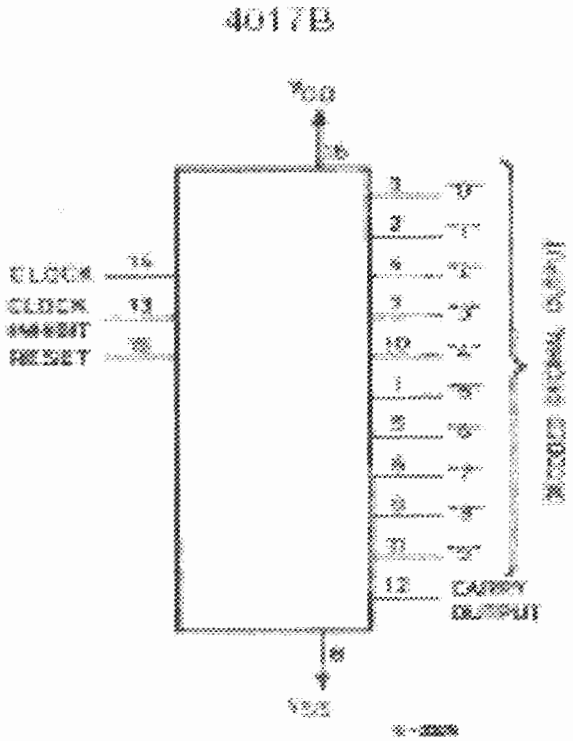


FIG. 9 Functional Diagram

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
VDD	Supply Voltage : **HCC** Types **HCF** Types	3 to 18 3 to 15	V V
VI	Input Voltage	0 to VDD	V
To p	Operating Temperature : **HCC** Types **HCF** Types	– 55 to + 125 – 40 to + 85	□C □C

LOGIC DIAGRAM

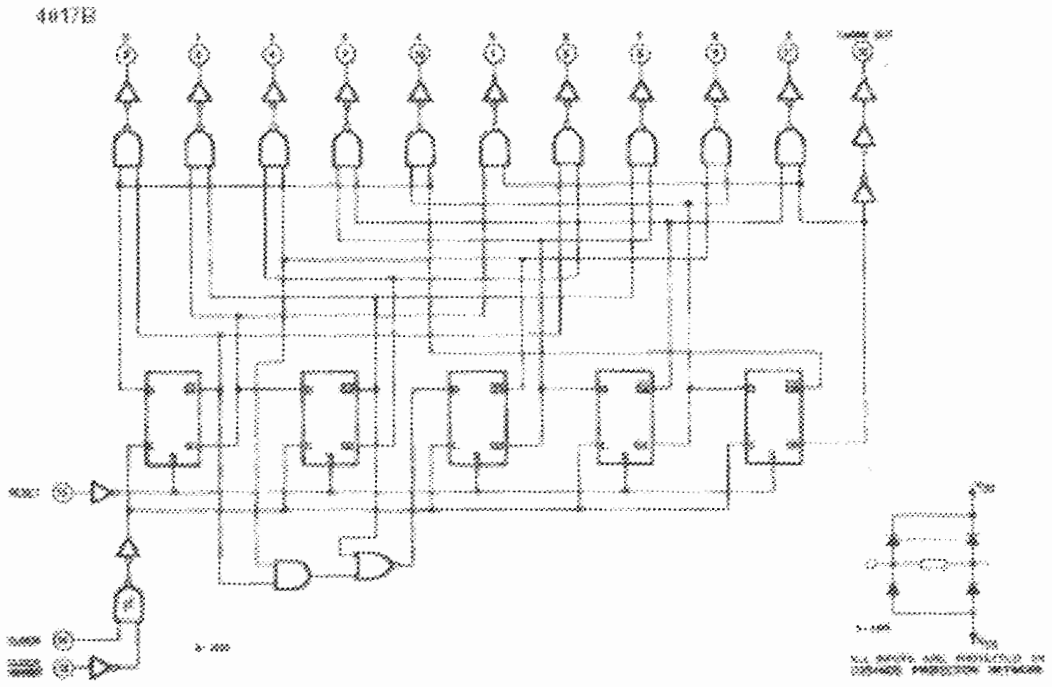


FIG. 10 Logic Diagram

TIMING DIAGRAM

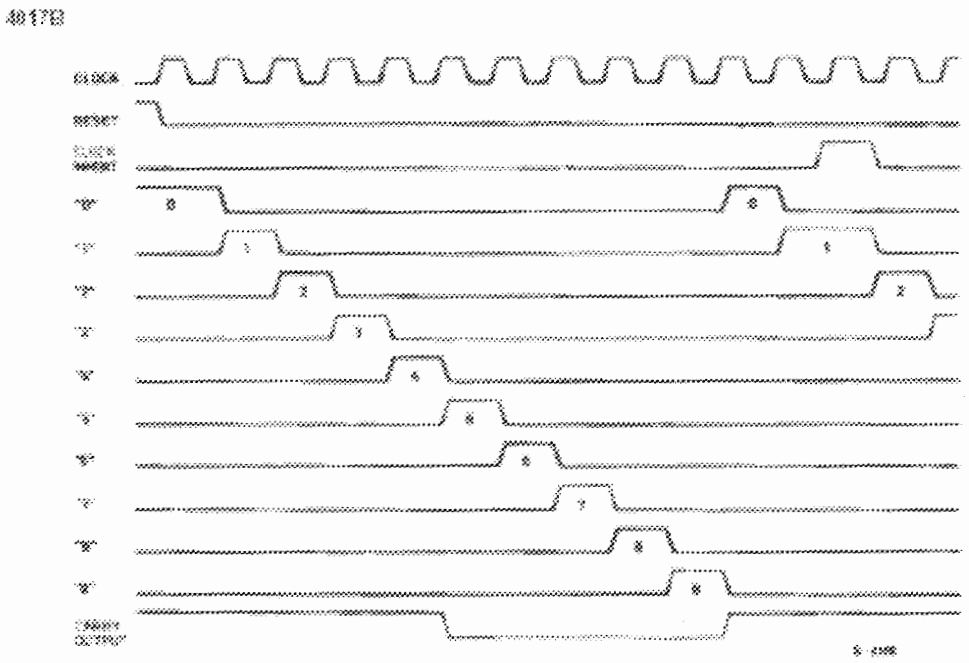


FIG. 11 Timing Diagram

TYPICAL APPLICATIONS

Divide by N Counter (N 3 10) with N Decoded Outputs. When the Nth decoded output is reached (Nth clock pulse) the S-R flip-flop (constructed from two NOR gates of the **HCC/HCF4001B**) generates a reset pulse which clears the **HCC/HCF4017B** to its zero count. At this time, if the Nth decoded output is greater than or equal to 6, the C-OUT line goes high to clock the next **HCC/HCF4017B** counter section. The "0" decoded output also goes high at this time coincidence of the clock low and decoded "0" output 0high resets the S-R flip flop to enable the HCC/**HCF4017B**. If the Nth decoded output is less than 6, the C-OUT line will not go high and, therefore, cannot be used. In this

case "0" decoded output may be used to perform the clocking function for the next counter.

CHAPTER THREE

3.0 CONSTRUCTION PROCEDURE.

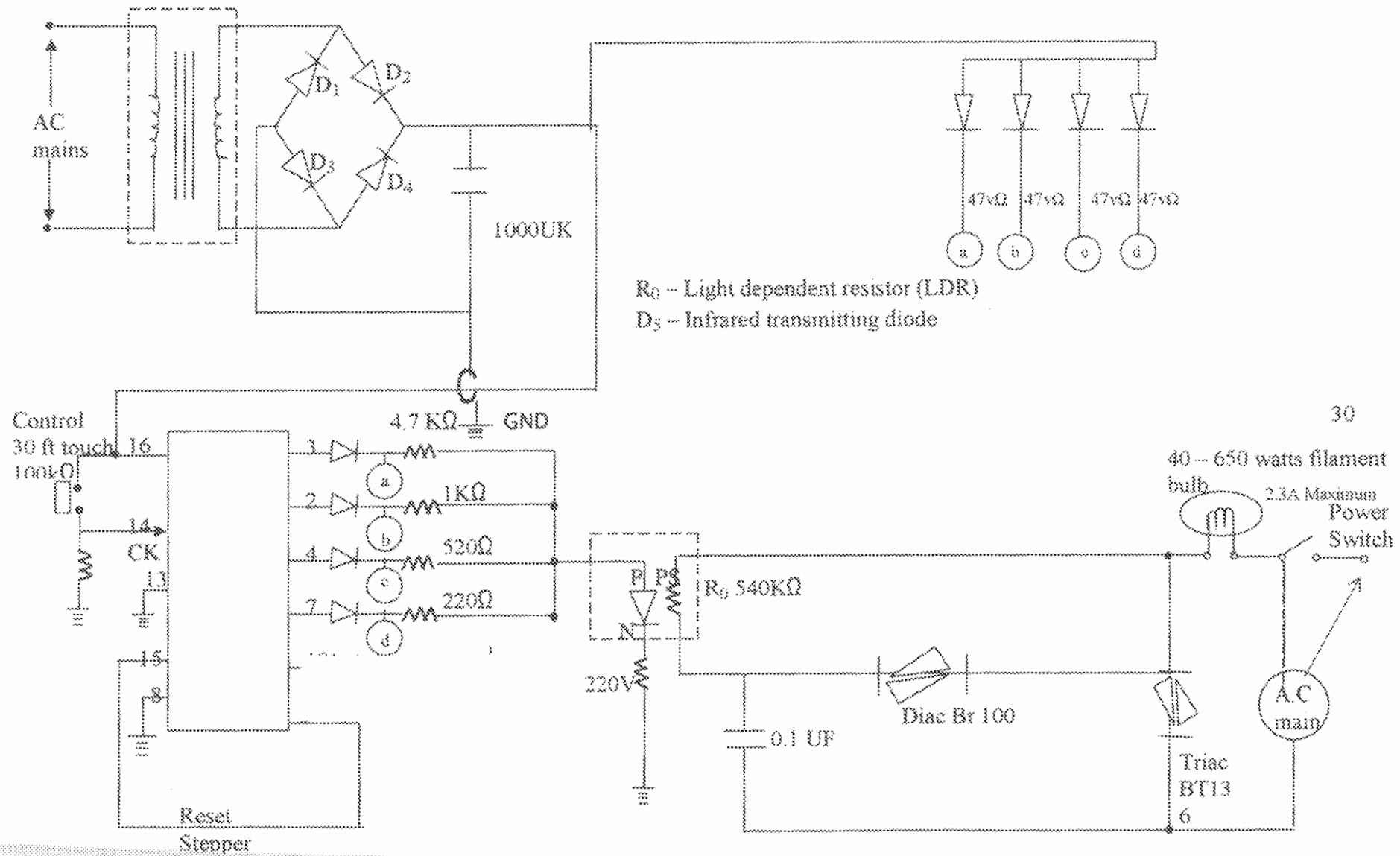
3.1 TESTING OF COMPONENTS

Prior the construction of the circuit, test were carried out on the components to be used such as transformer, resistor, diodes, [redacted]s are in good condition.

S/No	List of the component used	Quantity
1	Resistors	19
2	Diodes (Infrared Transmitting Diode)	1
3	Diodes	3
4	Light dependent resistor	1
5	1000uf 16v Capacitor	
6	Triac	1
7	Diac	1
8	Transformer	1
9.	Soft touch button	1

3.2 CONSTRUCTION

This project was formerly constructed on bread board and tested, later transferred to Vero-board in the same way the display circuit was built


AC
mains
D1
D2
D3
D4
1000UK
47vΩ
47vΩ
47vΩ
47vΩ
a
b
c
d
R0 – Light dependent resistor (LDR)
D5 – Infrared transmitting diode
4.7 KΩ
GND
Control
30 ft touch
100kΩ
16
14
CK
13
15
9
3
2
4
7
1KΩ
520Ω
220Ω
P1
P2
R0 540KΩ
220V
0.1 UF
Diac Br 100
Triac
BT13
6
30
40 – 650 watts filament
bulb
2.3A Maximum
Power
Switch
A.C
main
Reset
Stepper

as a separate unit before, it was been incorporated into the light dimmer circuit IC socket were used to avoid damage to chips due to excessive heat during soldering.

The cashing had a lamp – holder on which the test- bulb could be mounted and a socket outlet for connecting other loads.

3.3 TESTING OF THE DIMMER CIRCUIT.

Different level of attenuation where selected at R = 200kΩ the light came on and increased steadily to it's full brightness at 0kΩ.

Resistance (Ω)	Voltage (V)
0	220
50	170
100	120
150	75
200	40
250	0

4.0 CONCLUSION.

This project was specially designed to dim electric current. From the table of the result of the dimmer circuit, it is observed the voltage drop as the resistance has been increased, that is to say the aim of this project has been achieved.

RECOMMENDATION.

Regulator power supply may not be guarantee in Nigeria, I recommend that this project should be powered by a separate d.c power supply (e.g 12V battery).

If the project is to be developed for commercial purposes, provision must be made for it at the beginning of the construction for it to ensure the cable connection are well concealed.

4.2 REFERENCES.

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4) P. Horow and W . Hill. The Art of Electronic Cambridge University press 1010 price Edition 1998.