THE DESIGN AND CONSTRUCTION OF AUTOMATIC WATER PUMP CONTROLLER WITH LEVEL READ OUT

BY

OLAYEMI CHRISTOPHER OLUWOLE

2005/21975EE

DEPARTMENT OF ELECTRICAL/COMPUTER ENGINEERING, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA.

DECEMBER, 2009

THE DESIGN AND CONSTRUCTION OF AUTOMATIC WATER PUMP CONTROLLER WITH LEVEL READ OUT

BY
OLAYEMI CHRISTOPHER OLUWOLE
2005/21975EE

A THESIS SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING, FEDERAL UNIVERSITY OF TECHNOLOGY, MINNA.

DECEMBER, 2009.

DEDICATION

This project work is dedicated to the Almighty God, the giver of life from Whom all blessings flow.

DECLARATION

I, Olayemi Christopher Oluwole declare that this work was done by me and has never been presented elsewhere for the award of a degree. I also relinquish the copyright to the Federal University of Technology, Minna.

Olayemi Christopher O ..... Dr. E. N. Onwuka .....

(Name of Student) (Name of Supervisor)

....

(Signature and date) (Signature and date)

....

(Name of H.O.D) (Name of External Examiner)

....

(Signature and date) (Signature and date)

ACKNOWLEDGEMENT

I wish to acknowledge the immense efforts of others towards the successful completion of this project work.

My first gratitude goes to my wife Mrs. Victoria Olayemi for her moral support. I equally express my gratitude to my project supervisor, Dr. E.N. Onwuka for her professional and carrier guidance and for taking her time to effect necessary corrections on the project works.

Finally, my appreciation goes to the Head and all the lecturers of the Department of Electrical and Computer Engineering, Federal University of technology, Minna for their indispensable contributions to the project work.

ABSTRACT

The objective of this project is to design and construct a system that automatically monitors and controls water level in an overhead tank in order to ensure steady water supply and at the same time prevent water wastage through overflow. For ease of design and construction, the circuitry was broken down into smaller units called blocks. Each block was designed and tested and then assembled together to form the complete circuitry. The project can be used to monitor and maintain water level in overhead tank and reservoir of whatever capacity. However, the circuit cannot be used for purely non-conducting fluid. For non-conducting fluid, some modifications need to be made in the fluid level sensors. The circuit can however be kept intact.

LIST OF FIGURES

LIST OF TABLES

TABLE OF CONTENTS

CHAPTER ONE

1.0 Introduction

Water has always been essential to life on earth. Without it and the miracle of water cycle, we simply wouldn't survive. The strange thing however is that only one-percent of the water on our planet is available for treating and drinking [1]. Water is fundamental to all life on earth; while it may be easy for many of us to take the availability of water for granted; growing demands on the world's water resources highlight the importance of water to everyday life.

Man uses of water include agricultural, industrial, household, recreational, environmental activities [2]. The steady supply of water for man's use has become a thing of serious concern to man in recent times. Human therefore are generally settled near convenient source of water

The need therefore to build a means of control and steady supply of water for man's use especially household use cannot be over-emphasized. Hence the design and construction of the automatic digital water pump controller with level read -out.

The automatic water pump controller is used to control the water pump automatically. It switches on when water in an overhead tank falls below the lower limits. Similarly it gets switched off when the water tank is filled up.It also gives a read out of the level of water in the tank at various levels for effective monitoring of water levels in the tank.

Unlike most methods used to control water which are human dependent, the automatic water pump controller as an automatic control for a liquid pump assures that the pump starts pumping when the liquid reaches a predetermined level and the pump is stopped when the level has risen to a second predetermined level [3]. The automatic water

pump controller eliminates the need for any human manual switching of pumps installed for the pumping of water from a reservoir to an overhead tank [4].

The automatic water pump controller therefore saves water and energy, maintains water level and ensures the continuous supply of water while preventing overflowing and over pumping at the same time. This saves overhead cost and allows the user to be free from the bother of switching the water pump ON and OFF and makes water available throughout the day [5].

1.1 Objectives

The objective of this project is to design and construct a system that automatically monitors and control water level in an overhead tank in order to ensure steady water supply and at the same time prevent water wastage.

1.2 Scope of work

The circuitry can be used to monitor and maintain water level in overhead tank and reservoir of whatever capacity. However, the circuit cannot be used for purely non-conducting fluid. For non-conducting fluid, some modifications need to be made in the fluid level sensors. The circuit can however be kept intact [4].

1.3 Methodology and sources of materials

The complete circuit of the automatic water pump controller was split into unit blocks for ease of design and construction. Each unit block was assembled and tested on the breadboard prior to soldering on Vero board so as to ensure functionality of the entire circuit. I started with component testing after which bread boarding of each unit was done and necessary test were carried out and the entire circuit was finally assembled. The final circuit performance was in consonance with the project objectives.

The electronic components used for the project design and construction were obtained locally in the market. Electrical/electronic text books of varieties of authors as well as miscellaneous websites were consulted as referenced.

1.4 Overview of the design

The automatic digital water pump controller with level read-out consists basically of a regulated power supply unit, sensing switch unit, analog-to-digital converter unit, control unit and the pump actuator unit.

The sensing probes detects water level in the tank which then makes its contacts to close thereby making the output of a 555 timer in monostable mode to go high. The output stays high as long as it trigger (pin 2) is low. This voltage is sent to the analog-to-digital (ADC) which consists of an encoder and a decoder. The encoder produces a binary equivalent of the position of the level in the tank for the decoder which then produces the corresponding Binary-coded-decimal (BCD) to the display unit (seven segments) to display the water level in digital form. The control unit (CU) has the clock pulse generator incorporated in its circuit that automatically starts and stops the water pump via the pump actuators.

As a result of this detection and control, the water level in the tank will be known and maintained as long as there is power supply.

CHAPTER TWO

Literature review/theoretical background

2.0 Historical Background

There have been many developments in automatic control theory in recent years. The primary motivation for feedbacks control in times of antiquity was the need for the accurate determination of time. Thus in about 270, the Greek Ktesibios invented a float regulator for water clock. The function of this regulator was to keep the water level in a tank at constant depth. This constant depth yielded a constant flow of water through a tube at the bottom of the tank which filled a second tank at a constant rate. The level of water in the tank thus depended on time elapsed. The float regulator of Ktseibios used a float to control the inflow of water through a valve; as the level of water fell, the valve opened and replenished the reservoir; this float regulator performed the same function as the ball and clock in a modern flush toilet.

During the first century AD, Heron of Alexandria developed float regulators for water clocks. The Greek used the float regulators and similar devices for purposes such as automatic dispensing of wine, the design of siphons, maintaining constant water level differences between two tanks, the opening of temple doors e.t.c. In 800 through 1200, Arab engineers such as the three brothers Musa, Aljazari and Ibnal Saat used float regulators for water clocks and other applications. During this period, the important feedback principle of ON/OFF control was used which comes up again in connection with the minimum- time problems in the 1950's. When Baghdad fell to the Mongols in 1258, all creative thinking along these lines came to an end. Moreover, the invention of the mechanical clock in the 14th Century made the water clock and this feedback control system obsolete. (The mechanical clock is not a feed back control system).

The float regulator does not appear again until it is use in the industrial revolution.

It is worth mentioning that a pseudo feedback control system was developed in China in the 12th Century for navigational purposes. The South pointing chariot had a statue which was turned by a gearing mechanism attached to the wheels of the chariot so that it continuously pointed south. Using the directional information provided by the statue, the charioteer could steer a straight course. This is called a pseudo- feedback control system since it does not technically involve feedback unless the actions of the charioteer are considered as part of the system thus it is not automatic control systems.

In his book of 1746, W Salmon quoted prices for ball and cock float regulators used for maintaining the level of house water reservoirs – this regulator was used in the first patents for the flush toilet around 1775.

Thus automatic control system can be said to be dated back to the ancient water clock of Ktesibios earlier described – since then, a variety of automatic devices have been used to accomplish useful tasks or for entertainment. The latter include the automata popular in Europe in the 17th and 18th centuries featuring dancing figures that would repeat the task over and over again; these automata are examples of open – loop control. Milestones among feedback or closed loop automatic control devices, include temperature regulator of a furnace attributed to Debbel. Circa 1620 and the centrifugal flyball governor used for regulating the speed of steam engines by James Watt in 1788.

In his 1868 paper "on Governors", J.C. Maxwell (who discovered the Maxwell electromagnetic field equations) was able to explain instabilities exhibited by the fly ball governor using differential equations to describe the control system. This demonstrated the importance and usefulness of mathematical models and methods in understanding complex phenomena and signaled the beginning of mathematical control and system

theory. Elements of control theory had appeared earlier but not as dramatically and convincingly as in Maxwell's analysis.

Control theory made significant strides in the next 100 years – new mathematical techniques made it possible to control more accurately, significant more complex dynamic systems than the original fly ball governor. These techniques include developments in optimal control in the 1950s and 1960s followed by progress in stochastic, robust, adapted and optimal control methods in the 1970s and 1980s.

Application of automatic control in science and engineering today are very numerous ranging from process control, communication satellites, aircraft system to domestic application such as the automatic water pump controller. [6]

The earlier type of pump was the Archimedes screw type, first used by Sennacherib, king of Assyria for the water system at the hanging Gardens of Babylon and Nineveh in the 7th century BC and later described more in the 3rd century BC. In the 13th century AD, Ajiazari described and illustrated different types of pumps, including a reciprocating pump, double – action pump, suction pump and piston pump[7]. In Indian mythology, Lord Krishna playfully splashed colours on Goppes using a pichkaare which was and is now a reciprocating hand pump. Hence historically pichkaare should be recognized as the first ever pump.

The focus of this project is on automated pump named automatic water pump controller with level read-out. Similar projects have been of interest to my predecessors in the department and various works has been carried out on it namely:

-the design and construction of an overhead tank water level indicator and pump actuating device by Aweda .P. Olatunbosun [2000].

- the design and construction of automatic pump control unit system with audio-visual indicators by David .B.Nmadu[2003].

- the design and construction of a six steps water level indicator with a single decode light emitting diode(LED) by Raman Rabe[2003].
- the design and construction of water level indicator with audio alarm by Olayiwola Magaji[2008].

These previous project works used LED as water level indicator and some of them cannot automatically shutdown the pump at high water level. As a result of these, there is need for improvement on the previous works. In this project, instead of using LED indicators for the water level, a digital read out of the water levels is rather used and the pump controller is fully automated with the ability to start up and shutdown automatically depending on the water level in the overhead tank.

2.1 Seven-segment display.

A seven-segment display is a form of electronic display device for displaying decimal numerals. A seven segment display as its name indicates is composed of seven elements [8] and each segment in the display is a LED. By forward – biasing selected combinations of segments, any decimal digit and a decimal point can be formed [9]. The display may have 7, 8 or 9 leads on the chip. Usually leads 8 and 9 are decimal point [10]. The LED segment arrangement is shown below:

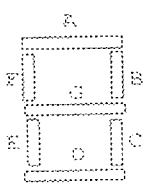


Fig 2.0 Led arrangement of seven segment Display

Two types of displays are available namely: the common anode and the common cathode.

The seven-segment LED has four individual digits each with a decimal point. Each of the seven-segments in a given digit contains an individual LED. When a suitable

voltage is applied to a given segment LED, current flows through and illuminates that segment LED by choosing which segment can be shown. The seven segments are arranged as a rectangle of two vertical segments on each side with one horizontal segment on the top, middle, and bottom [11].

2.2 Electromechanical relay.

Electromechanical relay are electromagnetically controlled mechanical device in which electrical contacts are opened or closed by a magnetizing current [12]. They are devices that complete or interrupt a circuit by physically moving electrical contacts into contact with each other. A relay involves two circuits: the energizing circuit and the contact circuit.

The coil is on the energizing side and the relay contacts are on the contact side. When a relay coil is energized, current flow through the coil creates a magnetic field; whether in a DC unit where the polarity is fixed or in an AC unit where the polarity changes 120 times per second, the basic function remains the same: the magnetic coil attracts a ferrous plate, which is part of the armature. One end of the armature is attached to the metal frame that is formed so that the armature can pivot while the other end opens and closes the contacts. Relays are extremely useful when we have a need to control a large amount of current and/or voltage with a small electrical signal[13].

Relay are switching devices typically used to control high power devices. In such relays the switching mechanism that is part of an operating circuit is activated by means of a relay solenoid through which the switching current flows [14].

2.3 Fixed three terminal regulators.

A voltage regulator provides a constant DC output voltage that is essentially independent of the input voltage, output load current and temperature. Most voltage regulators fall into two categories: linear regulators and switching regulators.

The most popular types of linear regulators are the three terminal regulators [15].A linear regulator is a voltage regulator based on an active device such as bipolar junction transistor operating in its linear region. The 78XX series regulates positive voltages whereas the 79XX series regulate negative voltages.The78XX series can supply up to 1.5A depending on the model [16]. The three terminals of fixed three terminal regulators are: the input, the output and the ground. The last two digits in the part number designated the output voltage. For example the 7805 is a +5.0 V regulator

There are only two important drawbacks of voltage regulator. First, the input voltage must be higher than the output voltage. Generally the input voltage must be at least 2V higher than the desired output voltage. The other problem is the excess voltage dissipated as heat and that is why it is attached to a heat sink. For protection, the regulators employ internal current limiting thermal shutdown, and safe-area compensation [17].

2.4 555 Timers

The 555 timer is one of the most popular and versatile integrated circuits ever produced. It includes 23 transistors, 2 diodes and 16 resistors on a silicon chip installed in an 8 – pin mini dual-in-line package [18]. The 8-pin 555 timer must be one of the most useful ICS ever made and it is used is used in many projects. With just a few external components it can be used to build many circuits not all of them involve timing [19].The pin configuration of 555 timer is shown on the next page:

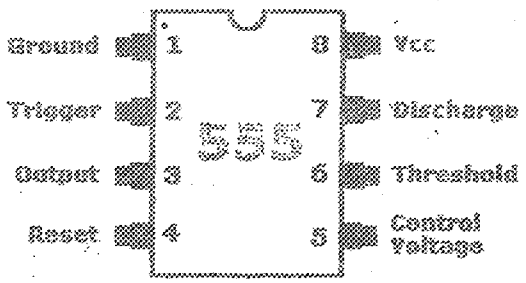


Fig 2.1 pin configuration of 555 timers

2.4.1 Operational mode of the 555 timer.

The 555 timer has two basic operational modes namely: as Monostable multivibrator and as astable multivibrator. A monostable multivibrator is said to have a single stable state that is the off state. Whenever it is triggered by an input pulse, the monostable switches to its temporary state. It remains in that state for a period of time determined by the RC network. It then returns to its stable state.

The other basic operational mode of the 555 is as astable multivibrator. An astable multivibrator is simply an oscillator. It generates a continuous stream of rectangular off – on pulses that switch between two voltage levels. The frequency of the pulses and their duty cycle are dependent upon the RC network values [20].

Other modes of operation of the 555 timer are bistable (flip-flop) which have two stable states and as inverting buffer (Schmitt trigger) in which the output logic state is the inverse of the input state.

2.4.2 Definition of pin functions.

Pin1 (Ground): The ground (or common) pin is the most negative supply potential of the device which is normally connected to the circuit common when operated from positive supply voltages.

Pin2 (Trigger): Is the input to the lower comparator and is used to set the latch which is turn causes the output to go high. This is the beginning of the timing sequence in monostable operation.

Pin3 (Output): this is the output of the 555 timer. The output of a standard 555 can sink and source up to 200mA. The output does not quite reach 0V or VCC in the low and high state respectively.

Pin4 (Reset): This pin is also used to reset the latch and return the output to a low state. The reset voltage threshold level is 0.7V and a sink current of 0.1mA from this pin is required to reset the device.

Pin5: (Control voltage): This pin allows direct access to the 1/3 +VCC, the reference level for the upper comparator. It also gives direct access to the lower comparator. The control input can used to adjust the threshold voltage which is internally set 2/3 +VCC. Usually this function is not required and the conurol input is connected to 0V with a 0.01uf.

Pin6 (Threshold): It is one of the inputs to the upper comparator and is used to reset the latch which causes the output to go low. It monitors the charging of the timing compactor of the astable and monostable circuits. It has a high input impedance > 10M

Pin7 [Discharge: This pin is not an input, it is connected to or when the timer output is low and is used to discharge the timing capacitor in astable and monostable circuit output.

Pin8 [+VCC]: The VCC is the positive supply voltage terminal of the 555 timer IC. The supply voltage ranges from +4.5v to 15v.

Table 2.0 555 timers' specifications.

Supply voltage (vcc)	4.5 to 15v
Supply current (vcc = 15v)	3 to 6mA
Supply current (vcc = +15v)	10 to 15mA
Output current (max)	200mA
Power dissipation	600mw
Operating temperature	0 to 70°c

2.5 Encoders.

An encoder can be a device used to change a signal (such as bit stream) of data into a code. The code serves any of a number of purposes such as compressing information for transmission or storage, encrypting of adding redundancies to the input code; or translating from one code to another. This is usually done by means of a programmed algorithm especially if a part is digital, while most analog encoding is done with analogue circuitry.

Encoder has 2^n input lines and n output lines. The output lines generate a binary code corresponding to the input value. The encoder has the limitation that only one input can be active at a time; if two inputs are simultaneously active, the output lines produces an undefined combination. To prevent this we make use of the priority encoder.

Priority encoders establish the priority of competing inputs by outputting a binary code representing the highest priority active input [21]. The encoder used in this project is 74LS148 and is a priority encoder.

2.6 Decoders.

A decoder is a device which does the reverse of an encoder undoing the encoding so that the original information can be retrieved [22]. It can take form of a multiple input, multiple-output logic circuit that converts coded inputs into coded output, where the input and output codes are different. Decoding is necessary in application such as data demultiplexing, seven-segment display, memory address decoding. A decoder circuit takes information presented in one form and converts into another form.

There are different kinds of decoders; there are decoders that convert binary numbers into BCD or BCD numbers into binary; some other ones convert BCD numbers into gray code. A common decoder circuit takes a BCD digit and converts into suitable driving signals for the seven segments LED display.

2.7 TTL Logic.

TTL stands for transistor-transistor logic ICS. Most TTL devices are designed to be operated from a well regulated power supply only. Higher or lower voltages will at best result in erratic operation and will more likely damage or destroy the semiconductor chips [23].

The logic levels of all the TTL products are fully compatible with each other. However, the input loading and output drive characteristic of each families is different and must be taken into consideration when using TTL families in a single system.

2.7.1 TTL Family.

Various TTL sub families exist and these include:

i. **Standard TTL:** 74XX series- it is the oldest logic, the most widely available and least expensive of all the logic family still in use. Its greatest advantage is low cost. Standard TTL offers moderate performance on both the power dissipation and delay

propagation ratings. A typical standard TTL gates dissipates about 10mw with a propagation delay of about 10ns.

ii. **Low power TTL:** 74LXX series – they are intended for application where power consumption must be kept at a minimum. The propagation delays are however higher and it is slow in operation.

iii. **Schottky TTL:** 74SXX series: it has higher switching speed and higher power consumption than the 74SLXX series and it is a good choice in applications where very high operating frequencies are used and a hefty power supply can provide ample current. A typical schottky TTL gate dissipates about 20mw but offers a propagation delay of 5ns.

iv. **Low – power schottky TTL:** 74LSXX series: It combines the advantages of both the 74LXX and 745XX series. The power dissipation is about 2mw with a delay propagation of 8ns. 74LSXX devices are significantly more expensive the previously covered sub – families.

v. **Advanced schottky TTL:** 74ASXX. Series- It has faster switching speeds than schottky TTL. The typical power dissipation for 74A5XX devices is about 4mw with propagation delay rating of about 1.5ns.

vi. **Advanced low-power schottky TTL:** 74ALSXX series- It combine the power dissipation of the 74LSXX series and the faster switching speed of the 74ASXX series. Typical power dissipation is 1mw but the propagation delay is 5ns. A 74ALSXX gate can be operated at frequencies

2.7.2 TTL Characteristics

i. **Supply voltage-** The bipolar TTL families require +5v + 5%.

ii. **Input:** A TTL input hold the low state sources current into whatever drives it (0.25mA a typical for LS) so to put it low you must sink current.

iii. **Output:** The TTL output stage is a saturated transistor to ground in the LOW state and a (Darlington) follower in the HIGH state.

iv. **Speed and power:** The bipolar TTL families consume considerable quiescent current. The corresponding speed go from about 25MHz (for Ls) to about 100MHz (for AS and F) [24].

The TTL ICs used in this used in this project are 74LSXX series namely 74LS47, 74LS148 and 74LS78.

2.8 Flip – Flops.

Flip – flops are memory elements with internal states as well external inputs. The output of a flip-flop depends on its internal state, which in turn, depends on the previous input of the flip-flop. [25] Each flip-flop has two outputs, Q and its complement.

The majority of flip flops are clocked and have a clock input which is used trigger the flip- flop.

2.8.1 Types of Flip-Flop

i. **The D Flip- Flop** – data flip flop is the easiest flip – flop to understand. D flip – flops have two inputs, D [data] input and a C [clock] input. The output of a D flip – flop is constant i.e. it remains in the previous state until its C input is clocked. When its C input is clocked, its Q output becomes equal to D until the next time it is clocked

ii **The RS Flip – Flop** – an RS flip – flop has two input, R [reset] and S [set] plus a third input C (clock) if it a clocked flip – flop. As long as both R and S are zero, the Q output

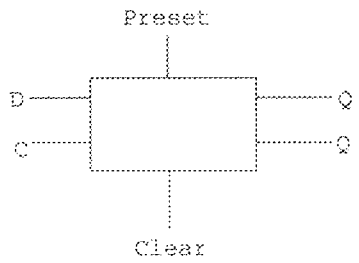


Fig 2.2 Schematic Diagram of D flip-flop

Table 2.1 Characteristic table of D flip-flop

D	$Q(t_{n+1})$
H	H
L	L

t_n D	t_{n+1} Q
H	H
L	L

of the RS flip – flop is constant and remains in its previous state. When R = 1 and S = 0, the Q output is forced to zero and remains at zero when R returns to zero.

When S = 1 and R = 0, the Q output is forced to one and remains at one when S returns to zero. The input conditions R = S = 1 should be avoided as it produces indeterminate state.

Fig 2.3 Schematic Diagram of D-Flip-flop.

Table 2.1 Characteristic Table of D flip-flop

		The State After	
$\bar{R}$	$\bar{S}$	Q	$\bar{Q}$
H	H	Q_n	$\bar{Q}_n$
L	H	L	H
H	L	H	L
L	L	Indeterminant	

iii **The JK Flip – Flop.** The JK flip – flop always has three inputs J,K and a clock input C. as long as a JK flip – flop is not clocked, it output is constant i.e. remains in the previous state. When a JK flip –flop is clocked, it behaves like an RS flip – flop [when J = R, K = S] for all input conditions except J = K = 1. if J = K = 0, the output does not change state. If J = 1 and K = 0, the Q output is reset to zero. If K = 1 and J = 0, the output is set to one. If both J and K = 1, the output change state (or toggles) each time it is clocked. The flip-flop used in this project is an edge-triggered J-K flip-flop.

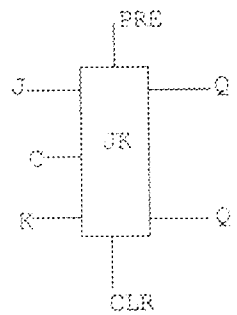


Fig 2.4 Schematic Diagram of the J-K flip-flop

Table 2.3 Characteristic table of J-K flip-flop

T_n					T_{n+1}
PRE	CLR	J	K	C	Q
L	H	X	X	X	H
H	L	X	X	X	L
L	L	X	X	X	Indeterminant
H	H	L	L	⎍⎍	Q_n No change
H	H	H	L	⎍⎍	H
H	H	L	H	⎍⎍	L
H	H	H	H	⎍⎍	

2.8.2 Edge Triggered Flip-flops.

An edge triggered flip – flop is clocked not by the level of the clock i.e. high or low, but by the transition of the clock signal from zero to one, or one to zero. The former case is called positive or rising – edge sensitive clock, and the latter is called a negative or

falling – edge sensitive clock. As the rising (or falling) edge of most pulses has duration of less than 5ns, an edge – triggered clock can be regarded as a level – sensitive clock triggered by a pulse of an infinitesimally short duration.

2.8.3 Flip – Flop Parameters.

To pick a flip – flop for some particular purpose, the following must be specified [26]

i. The logic family being used.

ii. The type of flip flop needed.

iii. The clocking type needed.

iv. The signs of the data inputs needed.

v. How many auxiliary inputs are needed?

vi. Timing constraints.

CHAPTER THREE

Design and Implementation.

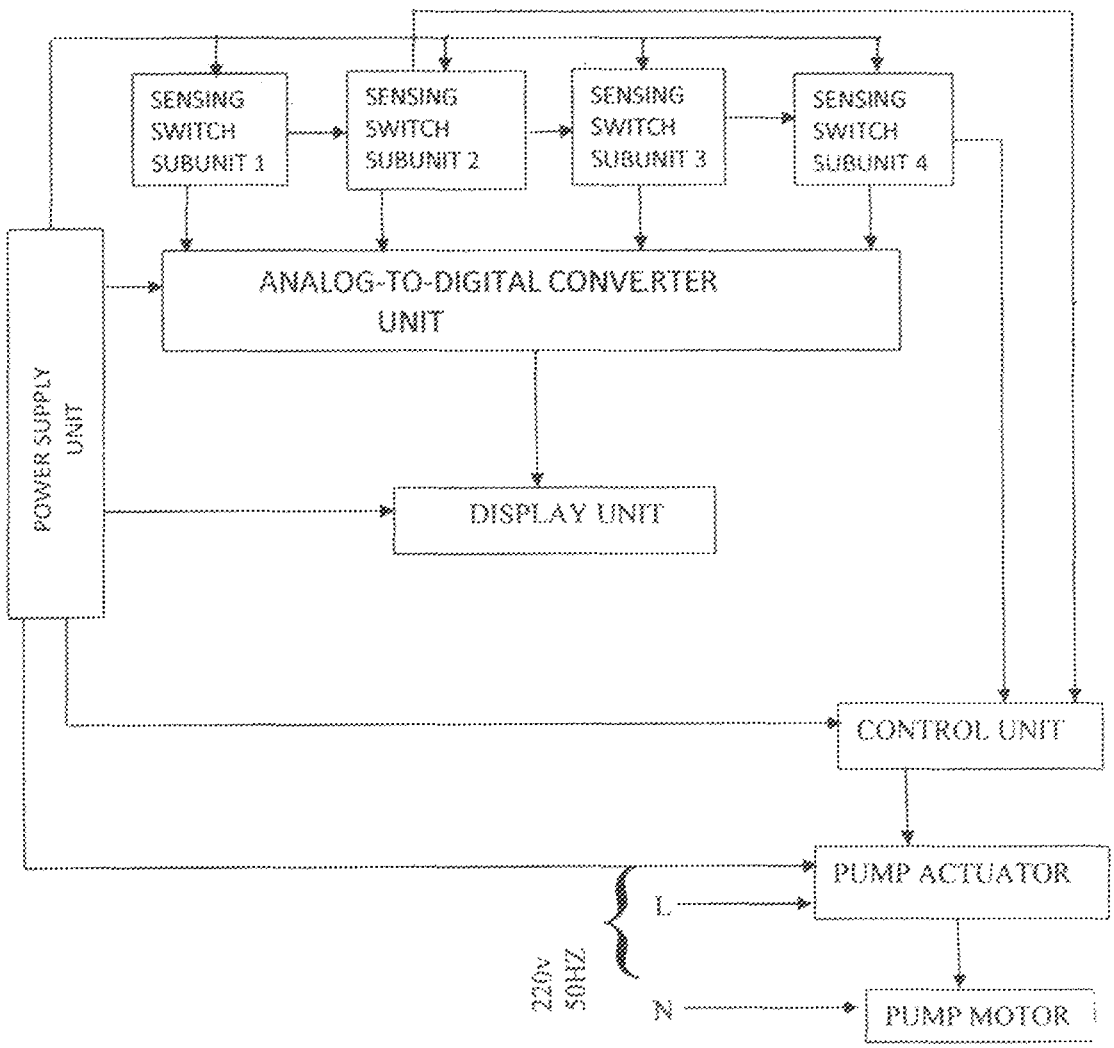


Fig 3.0 The block diagram of the of the automatic water pump Controller

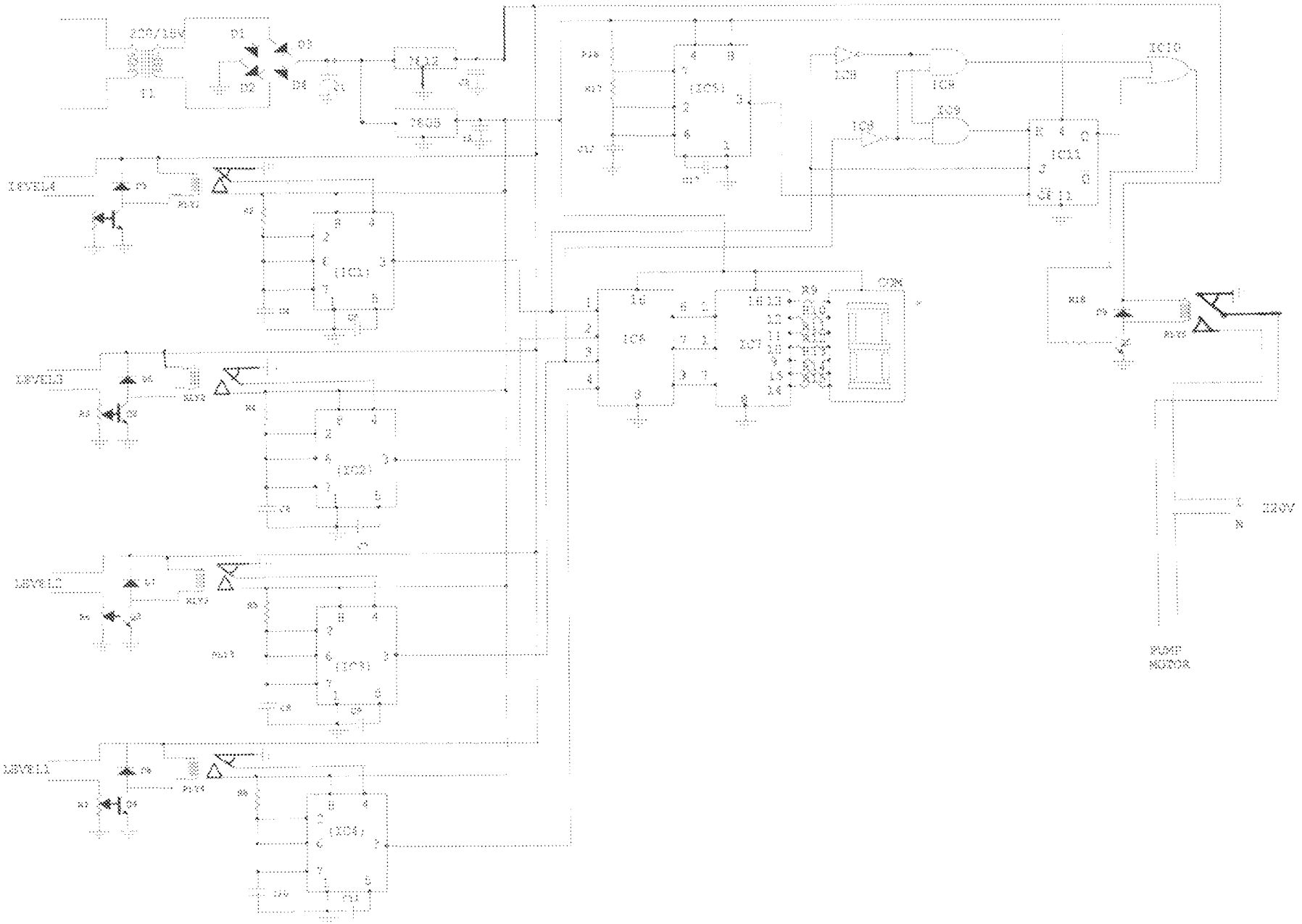


Fig 3.1. The complete circuit diagram of the of the automatic water pump controller

3.0 The power supply unit

The power supply unit is a regulated one. It consists of a step down transformer, a bridge rectifier, a filtering capacitor and three terminal regulators. The circuit diagram is as shown below:

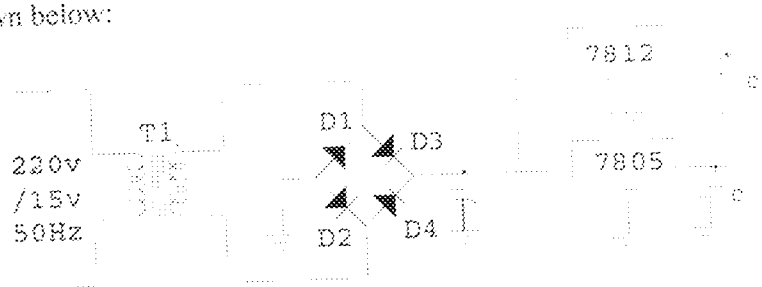


Fig 3.2 The power supply unit

The transformer steps down the supply voltage (220V AC) to the level required by the circuit (15V), the step down AC voltage is converted to a pulsating DC voltage by the bridge rectifier which consists of PN junction diodes. The filter capacitor smoothens the pulsating DC voltage by providing a low reactance path for alternating current and thereby suppresses ripple current[27]. The voltage regulators ensure that the terminal voltage is kept constant in spite of variation of load current. The voltage regulators in use are 7805 and7812 positive voltage regulators and they give Constant +5V and+12V respectively. The input voltage must be greater than output voltage by at least + 2V for proper regulation and the maximum current demand of the regulators is about 1A but can also be in excess of 1A when used with adaptor heat sink. The output capacitors act basically as a line filter to improve transient response.

3.1 The sensing switch unit.

The sensing switch unit consists of the sensing probes, 555 timer, a transistor and a DC relay. The diagram is as shown below:

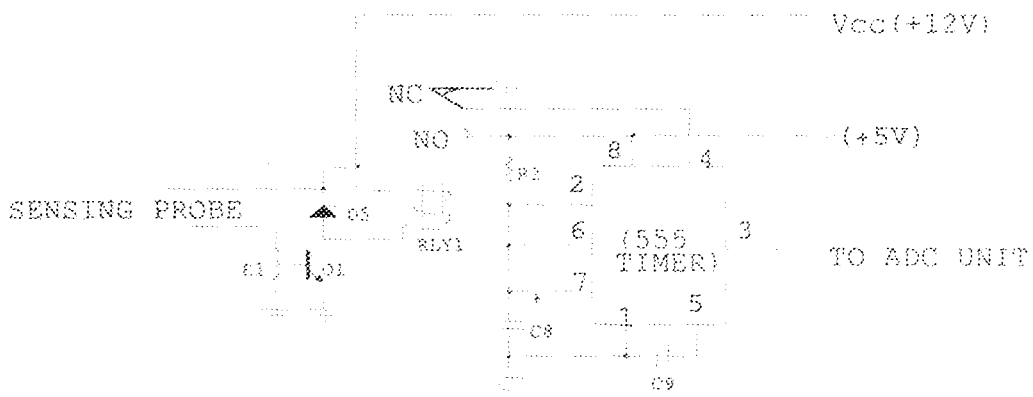


Fig 3.3 The sensing switch unit

The sensing switch unit detects water level in the tank via the sensing probes which consist of a normally open contact. When water is present, the contact of the sensing probes is closed and the transistor Q_1 goes to saturation and the relay is energized and this makes the reset pin of the 555 timer circuit in monostable mode to be at Vcc and the output of the 555 timer therefore goes high. This output voltage is sent to the analog – to digital converter and the display unit which displays the level in digital form. On the absence of water, Q_1 is cut off and the 555 timer reset (Pin 4) is at ground and hence the output (Pin 3) is also at ground (low). The diode protects the transistor from destruction due to back emf when the magnetic field of the relay coil collapses.

Using a 12V, 400Ω relay and Vcc = + 12V Q1 is an NPN transistor with part number C9014 and $hf_e = 50$

$Ic = Vcc/Rc = 12/400 = 0.03A$

Recall. $Ic = BI_B$ [28] and this is equal $hf_e . I_B$

$IB = Ic/hf_e = 0.03/50 = 0.6mA$ This is the base current required to saturate Q_1

$R1 = Vcc/ I_B = 12/ (0.0006) = 20K\Omega$

R1 was set at 20KΩ.

for the 555 timer, as long as its reset terminal (pin4) is at Vcc, its output (pin3) will remains high (approximately Vcc) but when the reset terminal (pin4) goes low or at ground due to the absence of water, the output (pin3) also goes low.

3.2 Analog – to – digital converter (ADC) unit

The output signal of the 555 timer of the sensing switch unit is an analogue signal. This is digitized by the ADC unit which makes use of the encoder and the decoder. The ADC circuit is as shown below:

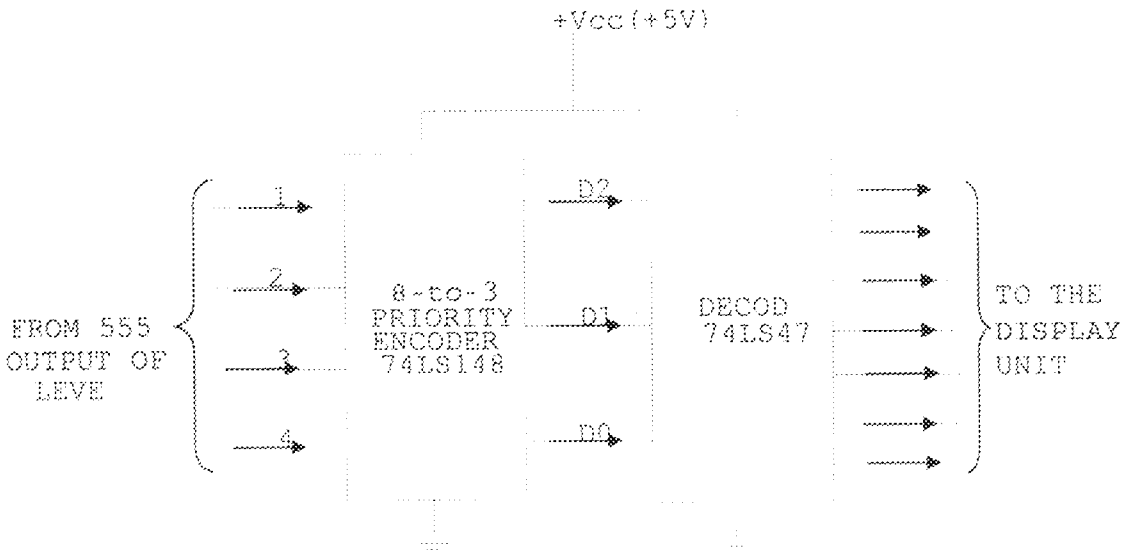


Fig 3.4 The Analog-to-digital converter unit

The encoder and the decoder used in the design is a TTL IC with their specifications as 74LS148 and 74LS47 respectively and these must powered with +5V supply. The 74LS148 encodes eight data lines to three line i.e. 4 – 2 –1 binary octal .The encoder is an 8 - to – 3 priority encoder and it produces the corresponding binary equivalent of the positions of the water level in the tank for the decoder which produces the corresponding binary coded decimal which is a suitable signal for driving the seven

segment display. The decoder accepts four lines of BCD {8, 4, 2, 1} input data, generates their complements internally and decodes the data to drive the seven segment display.

Table 3.0: ADC operation for 3 – bits

Binary encoder output	Decimal equivalent
D2 D1 D0	
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4

3.3 The digital display unit

The display unit is a seven segment which is a LED – based display. The diagram is shown below:

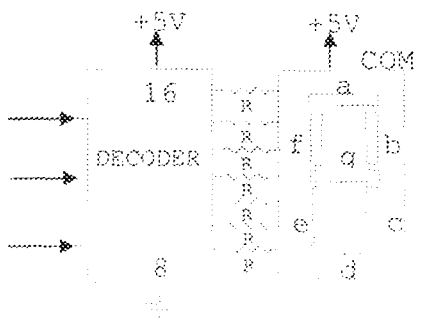


Fig 3.5 The Display unit

The driving signal for the display comes from the decoder. The seven segment display used is the common anode type since the output of the decoder is normally high. The resistors are current limiters.

With Vd=2V for each LED at 10mA,Vcc =+5v, we need to drop +3v for the LED to operate. Using Ohm's law, R=(Vcc-Vd)/I thus we have $(5\text{-}2)/10\text{x}10^{-3}$=300Ω.Thus R_9... R_{15} was chosen as 330Ω(standard value).

3.4 The Control unit

This is the very heart of the project. The control unit automatically starts and stops the motor via the pump actuator unit. The diagram is shown below:

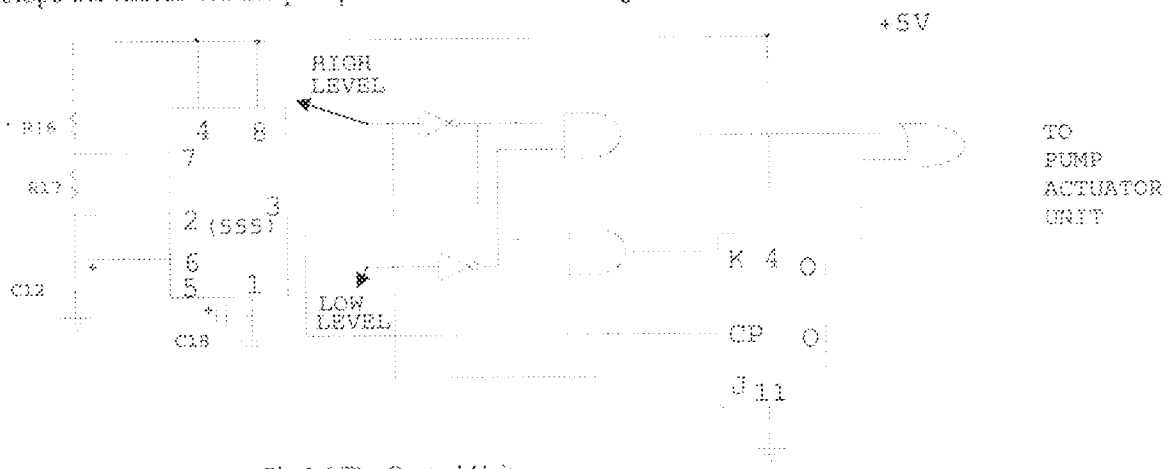


Fig 3.6 The Control Unit.

The control unit has two inputs and a clock input for clocking the negative – edge triggered J-K flip. The clock pulse generator which is a 555 timer connected in an astable mode provide the clock input necessary for adequate operation of the J-K flip flop. The free – running frequency of oscillation of the clock pulse generator is given by:

F=1.44/ (R1+2R2) C and the clock frequency requirement for 74LS78 is 0 – 30MHz [29]

The circuit of the clock pulse generator for the J-K flip-flop is shown below:

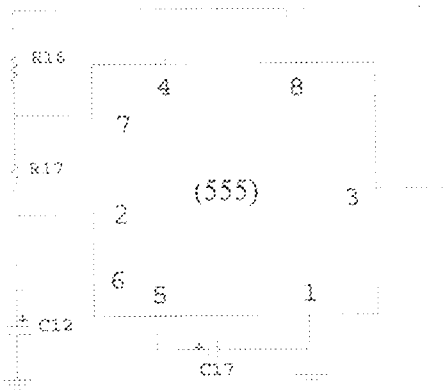


Fig 3.7 The clock pulse generator

R16 = 50KΩ, R17 = 10KΩ and C12 = 0.01μf

$F = 1.44/(R16+2R17)C = 1.44/(50x10^3+2x10x10^3)\ 0.01x10^{-6}$

$F = 2.057x10^4 Hz$=21 KHz=0.021MHz

Thus the frequency of the clock pulse generator for the J-K flip – flop is 0.021 MHz.

3.5 The pump actuator unit

The pump actuator unit serves as an interface circuit between the control unit and the pump motor. The unit controls the operation (start up and shut down) of the pump motor as directed by the control unit. The diagram of the pump actuator unit is shown below:

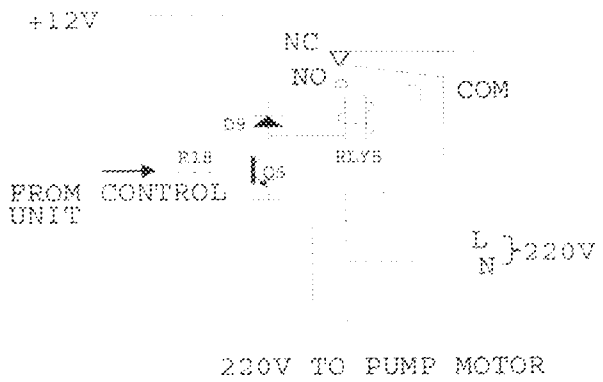


Fig 3.8 The pump actuator unit

The pump actuator unit consists of a DC relay and a transistor, the output signal from the control unit either saturates or cut off the transistor depending on the voltage level. When the transistor is saturated, the relay is energized and the pump starts and at cut off, the relay is de-energized and the pump shutdown. The diode is needed to protect the transistor from destruction due to back emf when the relay coil of the magnetic field collapses. When a coil is switched off a large back emf appears across the coil. This back emf may be several thousand volts in value which is enough to destroy the transistor.

The diode which is normally reverse biased is forward biased by the back emf and conducts its low resistance short-circuiting the back emf and protecting the diode [30]

CHAPTER FIVE

Conclusion and Recommendations

5.0 Conclusion

Automatic water pump controller is a feedback control system whose application ranges from domestic, industrial, to agricultural purposes. The design was in modular form, each module performing a specific task that forms an integral part of the entire system which automatically monitors and controls water level in an overhead tank via the activation/ the de-activation of water pump.

The design is only applicable to pump used for conducting fluid because the level sensor makes use of the conductivity of fluid to complete the circuit of the entire system.

5.1 Recommendations

In order to make the design more widely applicable as automatic pump controller, the following modifications may be made:

i) The DC Relay used in the sensing unit can be replaced with a two-way float switch which will makes the workability of the circuit independent of the conductivity of the liquid level being controlled.

ii) The system being an automated one, water must always be available in the reservoir in order to safeguard against dry running of the pump. In subsequent design, provision should be made in the circuit against the dry running of the pump.

Table 5.0 Bill of Quantity

S/N	COMPONENT	SPECIFICATION	DESCRIPTION	QTY	UNIT COST (₦)	AMOUNT
1	T1	220v/15v	Step down transformer	1	200	200
2	i. D1-D4	1N5401	P-N junction diode	4	30	120
	ii. D5- D8	IN914	Silicon diode	4	10	40
	iii.D9	IN4001	P-N junction diode	1	10	10
3	i. C1	3300µf, 25v	Electrolytic capacitor	1	100	100
	ii. C2, C3, C5, C7, C9.C11, C12	0.01µf	ceramic capacitor	7	30	210
	iii.C4, C6, C8, C10	0.022µf	Ceramic capacitor	4	30	120
4	i. R1,R3,R6,R7	0-100kΩ	Pre-set resistor	40	30	120
	ii. R2,R4,R5,R8	1MΩ	Carbon resistor	4	30	120
	iii.R9-R15	330Ω	Carbon resistor	7	20	140
	iv. R16	5k Ω	Carbon resistor	1	20	20
	v. R17	10k Ω	Carbon resistor	1	30	30
	vi.R18	0-50k Ω	Carbon resistor	1	30	30
5	RLY1 – RLY5	12v,400 Ω	Dc relay	5	120	600
6	i. 7805	7805	Fixed 3	1	60	60

			terminal			
	ii. 7812	7812	Voltage regulators	1	60	60
7	IC1 – IC5	NE 555	555 timer	5	100	500
8	IC6	74LS148	Encoder	1	150	150
9	IC7	74LS47	Decoder	1	150	150
10	IC8	74LS78	J-K Flip- flop	1	150	150
11	IC9 – 11	C4011	NAND Gate	3	120	360
12	Q1-Q5	C9014	Transistor	5	30	150
13	Casing		acrylic plastic			1000
14	Bread board			2	200	400
15	Vero board			1	150	150
16	Power switch	220vAC		1	60	60
17	Mic jack socket			5	60	300
18	Flexible cable	$1.5mm^2$		10 yards	70	700
19	Jumper wire			10 yards	50	500
20	Albro super glue			3	50	150
21	Silicon sealant			1	650	650
22	Incandescent lamp	60W,220V,50HZ		1	60	60
23	Lamp holder			1	60	60
24	water tap			1	300	300
25	Plastic container			1	150	150
26	Soldering lead			5 yards	20	100
27	Screw					150
			TOTAL			**8560**

5.2 REFERENCES

[1]www.stwater.co.uk/server.php?show=nav.00100006(Title:The history of water).

[2]www.en.wikipedia.org/wiki/water_resources(Title:water resources).

[3]www.freepatentsonline.com/5297939.html (Title: Automatic control for bilge and sump pump).

[4]www.electronics-lab.com/projects/sensors/027/ (Title: Economical pump controller).

[5]www.niagaraautomation.com(Title:Niagaraautomatic water pump controller).

[6]www.arri.uta.edu/acs/history.htm (Title:A brief history of automatic control:water clock for the Greek and Arabs).

[7]www.citizendia.org/Pump (Citizendia:pioneer pumps).

[8]www.en.wikipedia.org/wiki/seven-segment_display (Title: Seven segment display).

[9]Thomas.L.Floyd, Electronics devices, sixth edition, Pearson Education Inc.New Delhi, India, 2004, pp139.

[10]www.hibp.ecse.rpi.edu/~connor/education/EE/lectures/Lecture_7_digital_display.pdf(Title:Lecture 7 Digital display).

[11]www.answers.com/topic/seven-segment-display(Title:seven segment display;concept and visual structure).

[12]Thomas. L. Floyd, principles of electric circuit, fourth edition, prentice Hall inc. new jersey, USA .pp 968.

[13]www.allaboutcircuits.com/vol_4/chpt_5/1.html.(Title:Relay construction).

[14]www.electronics-manufacturers.com/products/relays-switches/electromechanical-relay/(Title:Electromechanical relay).

[15]Thomas L. Floyd, electronic devices, sixth edition, Pearson Education Inc. New Delhi, India; 2004. pp 139.

[16]www.en.wikipedia.org/wiki/linear_regulators(Title:Linear regulator;fixed regulators).

[17]www.rexfisher.com/All_Classes/Analog/78xx%20Voltage%20Regulator.pdf(Title:Three terminal positive voltage regulators:pp 1 of 16) .

[18]Forrest. M. Mims III. Engineer's mini-notebook 555 circuits, pp 4.

[19]www.Kpsec.FreeUk.com/555timer.htm(Title:555 and 556 timer).

[20]www.electronics.dit.ie/staff/mtully/555%20folder/555%20timer.htm.(Title.The 555 timer).

[21]www.en.wikipedia.org/wiki/encoder(Title:Encoder:Examples:the encoder circuit)

[22]www.en.wikipedia.org/wiki/decoder (Title:decoder)

[23]The master IC cookbook. Third edition, MC Graw-Hill, USA. 1997 PP 1

[24]Paul Horowitz and Winfield Hill, Art of Electronics, Cambridge university press, Great Britain. 1995. PP 486

[25]Allan Clements, principles of Computer Hardware, oxford university London. 1999 PP 99

[26]William. L. Faissler. An introduction to modern electronics, USA. 1991, PP 184

[27]www.answers.com/topic/filter-capacitor(Title:wikipaedia:filter capacitor).s

[28]B.L Theraja and A.K Theraja, A textbook of electrical technology, S.chand &company Ltd. New Delhi. India, 2001, pp 1756.

[29]www.it.lth.se/datablad/Logik/74LS/74LS78.pdf(Title:Recommended condition; pp 3 of 5(clock frequency).

[30]www.hobbyprojects.com/the_diode/diode_protection_circuits.html(Title:diode protection circuits Tutorial; diagram A).

APPENDIX

User's Manual

Please read the following instructions before switching on the appliance.

1) To avoid the risk of electric shock, do not operate the appliance when its casing is opened.
2) Connect the sensing probes from the water tank and the pump motor to their respectively jack socket as provided on the appliance.
3) As a guide for (2) above, see the labeling on the rear of the appliance's casing.
4) Ensure the necessary connections are properly done before putting the appliance into use.
5) For testing purpose, the filling up of the water tank should be done from the side of the tank opposite the level sensors' position in order to prevent making(closing) all the level sensors simultaneously which will lead to incorrect level read out.

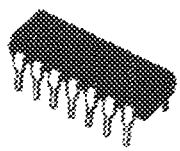
SGS-THOMSON MICROELECTRONICS

HCC4011B/12B/23B
HCF4011B/12B/23B

NAND GATES

QUAD 2 INPUT HCC/HCF 4011B
DUAL 4 INPUT HCC/HCF 4012B
TRIPLE 3 INPUT HCC/HCF 4023B

- PROPAGATION DELAY TIME = 60ns (typ.) AT C_L = 50pF, V_{DD} = 10V
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- INPUT CURRENT OF 100nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- 5V, 10V AND 15V PARAMETRIC RATINGS
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N°. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"



EY
(Plastic Package)

F
(Ceramic Frit Seal Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

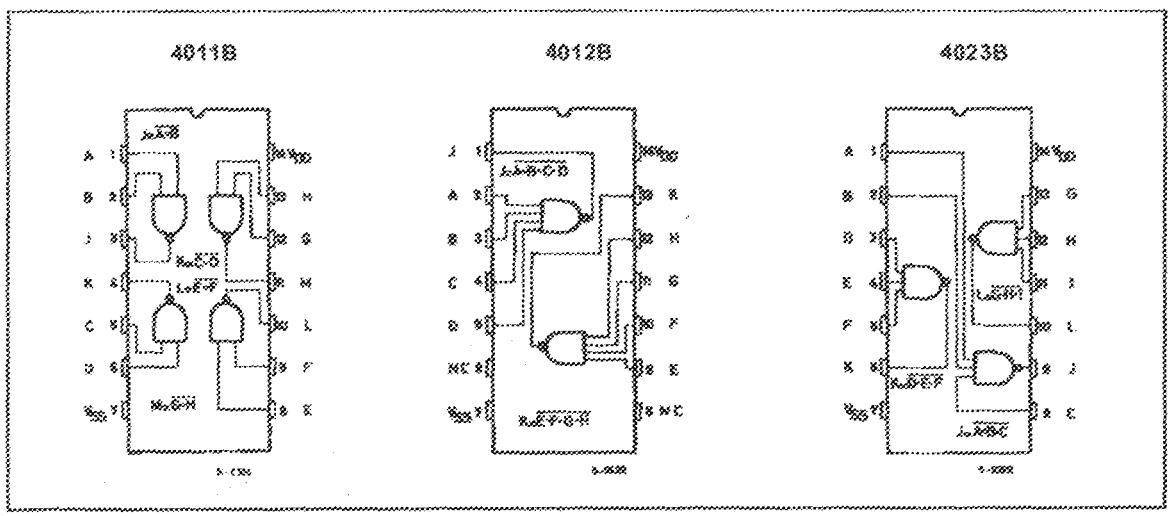
HCC40XXBF	HCF40XXBM1
HCF40XXBEY	HCF40XXBC1

DESCRIPTION

The **HCC4011B**, **HCC4012B** and **HCC4023B** (extended temperature range) and **HCF4011B**, **HCF4012B** and **HCF4023B** (intermediate temperature range) are monolithic, integrated circuit, available in 14-lead dual in-line plastic or ceramic package and plastic micropackage.

The **HCC/HCF4011B**, **HCC/HCF4012B** and **HCC/HCF4023B** NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

PIN CONNECTIONS



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Symbol	Parameter		Test Conditions V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	Value T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_L	Quiescent Current	HCC Types	0/5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
		HCF Types	0/ 5			5		1		0.01	1		7.5	
			0/10			10		2		0.01	2		15	
			0/15			15		4		0.01	4		30	
V_{OH}	Output High Voltage		0/5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output Drive Current	HCC Types	0/5	2.5		5	– 2		– 1.6	– 3.2		– 1.15		mA
			0/5	4.6		5	– 0.64		– 0.51	– 1		– 0.36		
			0/10	9.5		10	– 1.6		– 1.3	– 2.6		– 0.9		
			0/15	13.5		15	– 4.2		– 3.4	– 6.8		– 2.4		
		HCF Types	0/5	2.5		5	– 1.53		– 1.36	– 3.2		– 1.1		
			0/5	4.6		5	– 0.52		– 0.44	– 1		– 0.36		
			0/10	9.5		10	– 1.3		– 1.1	– 2.6		– 0.9		
			0/15	13.5		15	– 3.6		– 3.0	– 6.8		– 2.4		
I_{OL}	Output Sink Current	HCC Types	0/5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input Leakage Current	HCC Types	0/18	Any Input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
		HCF Types	0/15			15		± 0.3		$\pm 10^{-5}$	± 0.3		± 1	
C_I	Input Capacitance			Any Input						5	7.5			pF

* T_{Low} = – 55°C for HCC device : – 40°C for HCF device.
* T_{High} = + 125°C for HCC device : + 85°C for HCF device.
The Noise Margin for both "1" and "0" level is : 1V min. with V_{DD} = 5V, 2V min. with V_{DD} = 10V, 2.5V with V_{DD} = 15V.

ESCRIPTION

e 555 monolithic timing circuit is a highly stable controller capable producing accurate time delays, or oscillation. In the time delay ode of operation, the time is precisely controlled by one external sistor and capacitor. For a stable operation as an oscillator, the e running frequency and the duty cycle are both accurately ntrolled with two external resistors and one capacitor. The circuit y be triggered and reset on falling waveforms, and the output ucture can source or sink up to 200 mA.

EATURES

- Turn-off time less than 2 µs
- Max. operating frequency greater than 500 kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

PIN CONFIGURATION

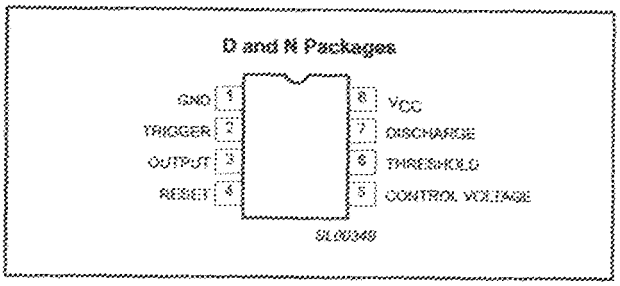


Figure 1. Pin configuration

BLOCK DIAGRAM

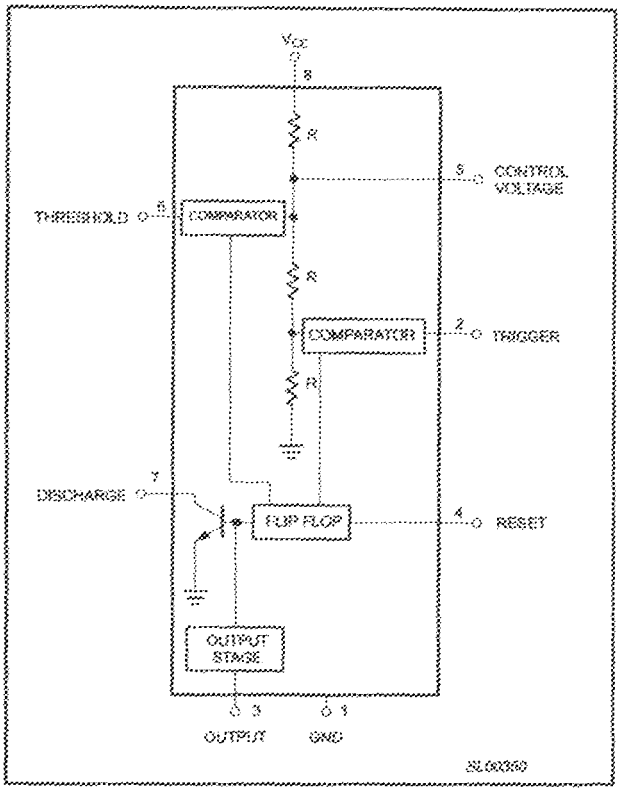


Figure 2. Block Diagram

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70 °C	NE555D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70 °C	NE555N	SOT97-1
8-Pin Plastic Small Outline (SO) Package	–40 °C to +85 °C	SA555D	SOT96-1
8-Pin Plastic Dual In-Line Package (DIP)	–40 °C to +85 °C	SA555N	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	–55 °C to +125 °C	SE555CN	SOT97-1
8-Pin Plastic Dual In-Line Package (DIP)	–55 °C to +125 °C	SE555N	SOT97-1

C AND AC ELECTRICAL CHARACTERISTICS

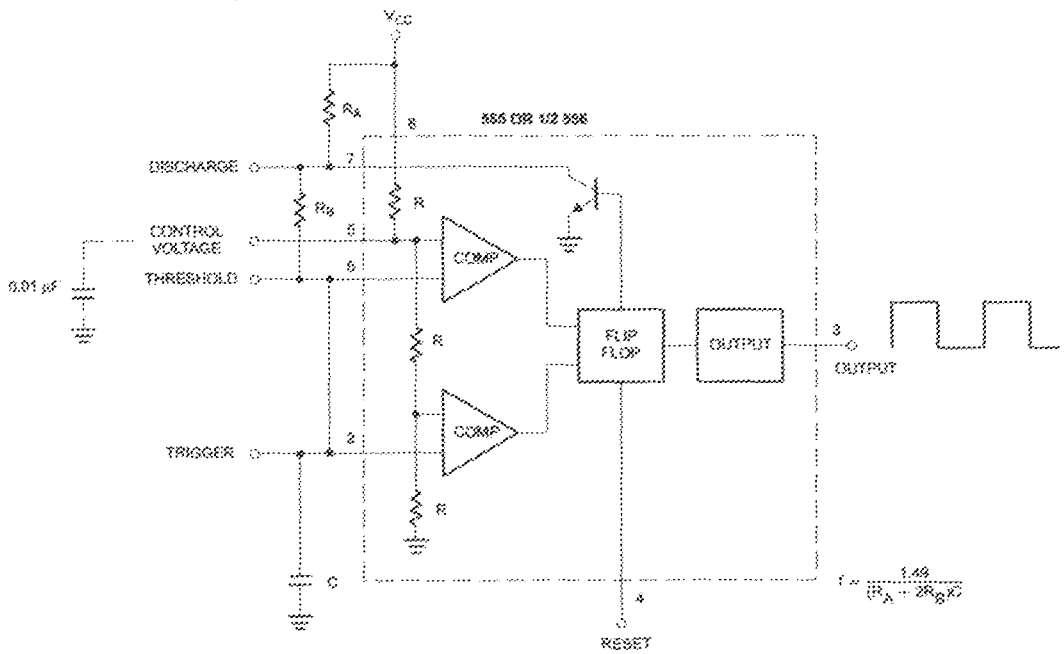
T_{amb} = 25 °C, V_{CC} = +5 V to +15 V unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SA555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
$_{CC}$	Supply voltage		4.5		18	4.5		16	V
$_{CC}$	Supply current (low state)[1]	V_{CC} = 5 V, R_L = ∞ V_{CC} = 15 V, R_L = ∞		3 10	5 12		3 10	6 15	mA mA
$_{it}$ $\Delta_M/\Delta T$ $\Delta_M/\Delta V_S$	Timing error (monostable) Initial accuracy[2] Drift with temperature Drift with supply voltage	R_A = 2 kΩ to 100 kΩ C=0.1 µF		0.5 30 0.05	2.0 100 0.2		1.0 50 0.1	3.0 150 0.5	% ppm/°C %/V
$_A$ $\Delta_A/\Delta T$ $\Delta_A/\Delta V_S$	Timing error (astable) Initial accuracy[2] Drift with temperature Drift with supply voltage	R_A, R_B = 1 kΩ to 100 kΩ C = 0.1 µF V_{CC} = 15 V		4 0.15	6 500 0.6		5 0.3	13 500 1	% ppm/°C %/V
V_C	Control voltage level	V_{CC} = 15 V V_{CC} = 5 V	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
V_{TH}	Threshold voltage	V_{CC} = 15 V V_{CC} = 5 V	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	µA
V_{TRIG}	Trigger voltage	V_{CC} = 15 V V_{CC} = 5 V	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
I_{TRIG}	Trigger current	V_{TRIG} = 0 V		0.5	0.9		0.5	2.0	µA
V_{RESET}	Reset voltage[4]	V_{CC} = 15 V, V_{TH} = 10.5 V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current Reset current	V_{RESET} = 0.4 V V_{RESET} = 0 V		0.1 0.4	0.4 1.0		0.1 0.4	0.4 1.5	mA mA
V_{OL}	LOW-level output voltage	V_{CC} = 15 V I_{SINK} = 10 mA I_{SINK} = 50 mA I_{SINK} = 100 mA I_{SINK} = 200 mA		0.1 0.4 2.0 2.5	0.15 0.5 2.2		0.1 0.4 2.0 2.5	0.25 0.75 2.5	V V V V
		V_{CC} = 5 V I_{SINK} = 8 mA I_{SINK} = 5 mA		0.1 0.05	0.25 0.2		0.3 0.25	0.4 0.35	V V
V_{OH}	HIGH-level output voltage	V_{CC} = 15 V I_{SOURCE} = 200 mA I_{SOURCE} = 100 mA	 13.0	12.5 13.3		 12.75	12.5 13.3		V V
		V_{CC} = 5 V I_{SOURCE} = 100 mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	V_{RESET} = V_{CC}		0.5	2.0		0.5	2.0	µs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

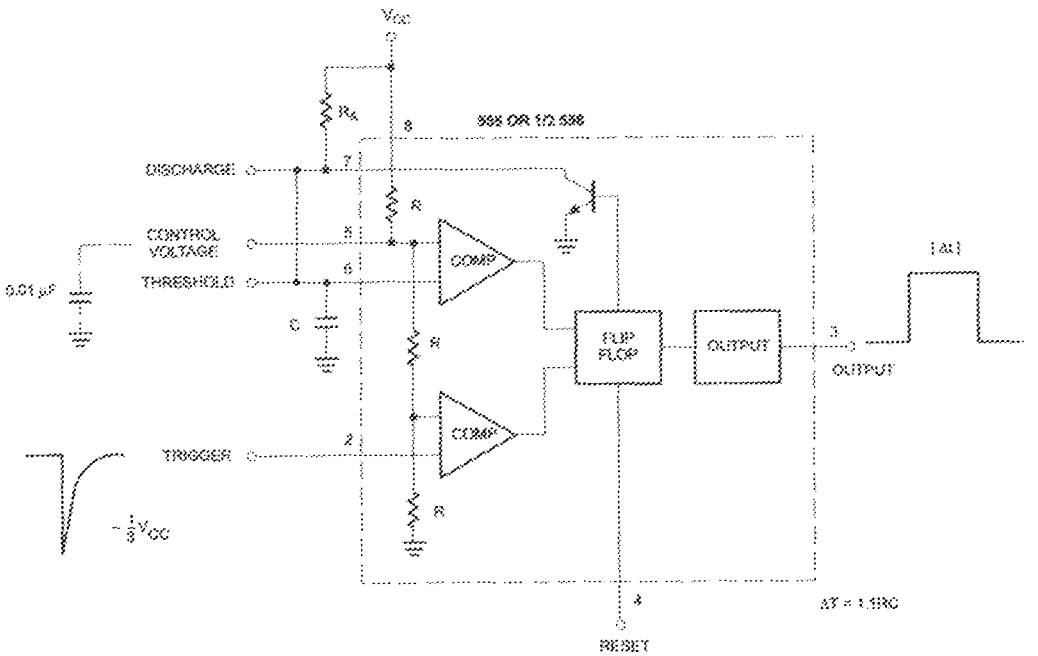
NOTES:

1. Supply current when output high typically 1 mA less.
2. Tested at V_{CC} = 5 V and V_{CC} = 15 V.
3. This will determine the max value of R_A+R_B, for 15 V operation, the max total R = 10 MΩ, and for 5 V operation, the max. total R = 3.4 MΩ.
4. Specified with trigger input HIGH.
5. Time measured from a positive-going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from HIGH to LOW of the output. Trigger is tied to threshold.

TYPICAL APPLICATIONS



Astable Operation



Monostable Operation

SL00393

Figure 8. Typical Applications

TYPES SN54H78, SN54L78, SN54LS78A, SN74H78, SN74LS78A
DUAL J–K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

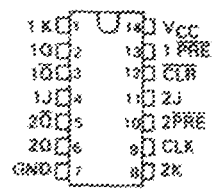
The 'H78 and 'L78 contain two J-K flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The 'H78 and 'L78 are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS78A contain two negative-edge-triggered flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The logic levels at the J and K inputs may be allowed to change while the clock pulse is high and the flip-flop will perform according to the function table as long as minimum setup and hold times are observed. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN54H78, SN54L78, and the SN54LS78A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74H78 and the SN74LS78A are characterized for operation from 0°C to 70°C.

FOR CHIP CARRIER INFORMATION, CONTACT THE FACTORY

SN54H78 . . . J PACKAGE
SN74H78 . . . J OR N PACKAGE
(TOP VIEW)



SN54L78 . . . J PACKAGE
SN54LS78A . . . J OR W PACKAGE
SN74LS78A . . . D, J OR N PACKAGE
(TOP VIEW)

'H78, 'L78
FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	⊓↓	L	L	Q_0	$\bar{Q}_0$
H	H	⊓↓	H	L	H	L
H	H	⊓↓	L	H	L	H
H	H	⊓↓	H	H	TOGGLE	

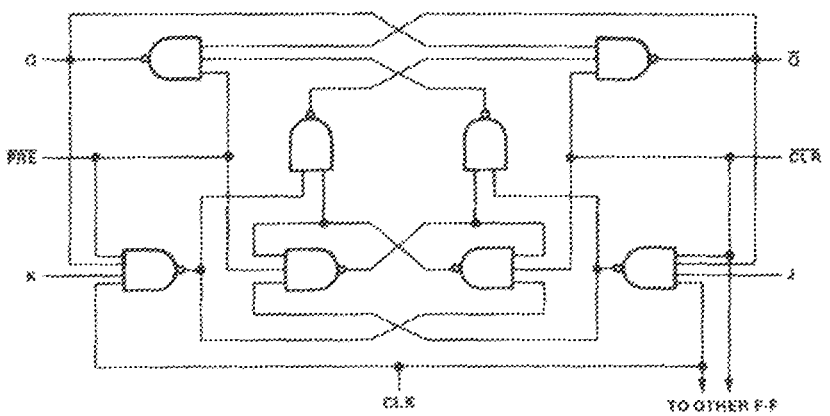
'LS78A

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

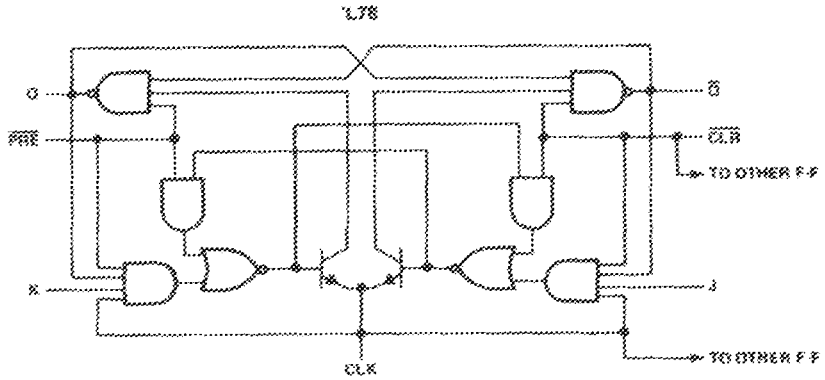
† This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

logic diagrams

'H78



'L78



TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54LS78A			SN74LS78A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		30	MHz
t_w	Pulse duration	CLK high	20			20			ns
		PRE or CLR low	25			25			
t_{su}	Setup time before CLK↓	data high or low	20			20			ns
		PRE or CLR inactive	20			20			
t_h	Hold time-data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS78A			SN74LS78A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = 0.7 V,	2.5	3.4					V
		V_{CC} = MIN, I_{OH} = −0.4 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,				2.7	3.4		
V_{OL}		V_{CC} = MIN, I_{OL} = 4 mA	V_{IL} = MAX,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 8 mA	V_{IL} = MAX,	V_{IH} = 2 V,					0.35	0.5	
I_I	J or K	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
	CLR						0.6			0.6	
	PRE						0.3			0.3	
	CLK						0.8			0.8	
I_{IH}	J or K	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
	CLR						120			120	
	PRE						60			60	
	CLK						160			160	
I_{IL}	J or K	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
	CLR						−1.6			−1.6	
	PRE						−0.8			−0.8	
	CLK						−1.6			−1.6	
I_{OS}§		V_{CC} = MAX,	See Note 4		−20		−100	−20		−100	mA
I_{CC}		V_{CC} = MAX,	See Note 2			3	6		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

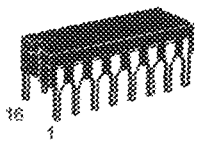
MOTOROLA

10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

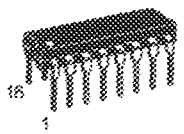
SN54/74LS147
SN54/74LS148
SN54/74LS748

10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

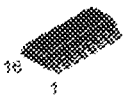
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

The SN54/74LS147 and the SN54/74LS148 are Priority Encoders. They provide priority decoding of the inputs to ensure that only the highest order data line is encoded. Both devices have data inputs and outputs which are active at the low logic level.

The LS147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition does not require an input condition because zero is encoded when all nine data lines are at a high logic level.

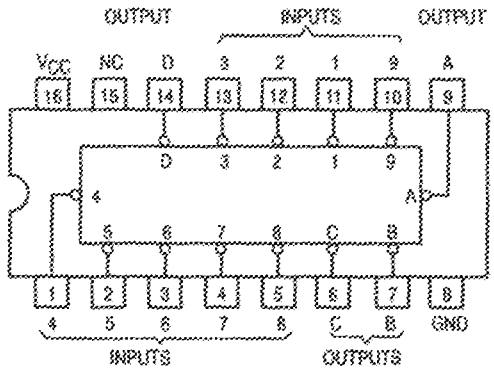
The LS148 encodes eight data lines to three-line (4-2-1) binary (octal). By providing cascading circuitry (Enable Input EI and Enable Output EO) octal expansion is allowed without needing external circuitry.

The SN54/74LS748 is a proprietary Motorola part incorporating a built-in deglitcher network which minimizes glitches on the GS output. The glitch occurs on the negative going transition of the EI input when data inputs 0–7 are at logical ones.

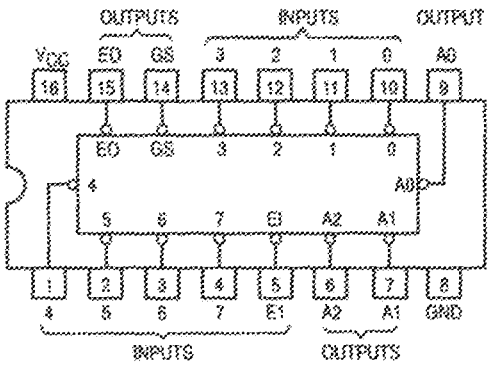
The only dc parameter differences between the LS148 and the LS748 are that (1) Pin 10 (input 0) has a fan-in of 2 on the LS748 versus a fan-in of 1 on the LS148; (2) Pins 1, 2, 3, 4, 11, 12 and 13 (inputs 1, 2, 3, 4, 5, 6, 7) have a fan-in of 3 on the LS748 versus a fan-in of 2 on the LS148.

The only ac difference is that t_{PHL} from EI to EO is changed from 40 to 45 ns.

SN54/74LS147
(TOP VIEW)



SN54/74LS148
SN54/74LS748
(TOP VIEW)



SN54/74LS147
FUNCTION TABLE

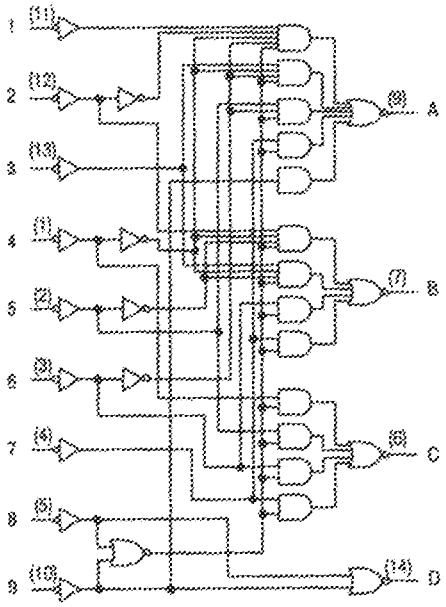
INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Logic Level, L = LOW Logic Level, X = Irrelevant

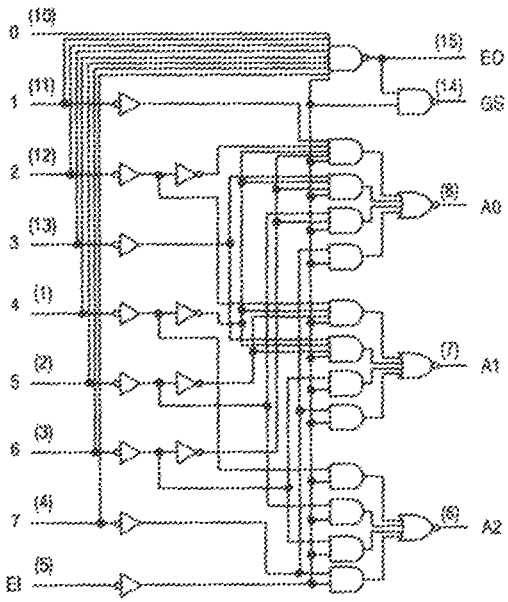
SN54/74LS148
SN54/74LS748
FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

FUNCTIONAL BLOCK DIAGRAMS



SN54/74LS147



SN54/74LS148

UARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

C CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current All Others Input 0 (LS748) Inputs 1–7 (LS148) Inputs 1–7 (LS748)				20 40 40 80	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	All Others Input 0 (LS748) Inputs 1–7 (LS148) Inputs 1–7 (LS748)				0.1 0.2 0.2 0.3	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current All Others Input 0 (LS748) Inputs 1–7 (LS148) Inputs 1–7 (LS748)				−0.4 −0.8 −0.8 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CCH}	Power Supply Current Output HIGH				17	mA	V_{CC} = MAX, All Inputs = 4.5 V	
I_{CCL}	Output LOW				20	mA	V_{CC} = MAX, Inputs 7 & E1 = GND All Other Inputs = 4.5 V	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

FAIRCHILD
SEMICONDUCTOR™

October 1988
Revised March 2000

DM74LS47
BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

General Description

The DM74LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 µA. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions.

Features

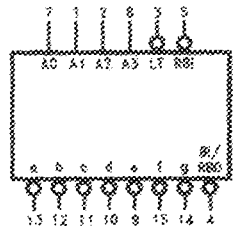
- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

Ordering Code:

Order Number	Package Number	Package Description
DM74LS47M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS47N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

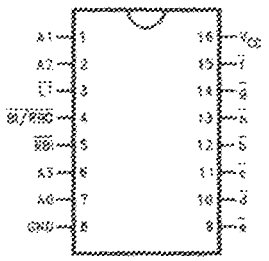
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Connection Diagram



Pin Descriptions

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI/RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$ – $\overline{g}$	Segment Outputs (Active LOW) (Note 1)

Note 1: OC—Open Collector

Truth Table

Decimal or Function	Inputs							Outputs							Note
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 2)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 2)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 3)
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 4)
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 5)

Note 2: $\overline{BI/RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 3: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

Note 4: When ripple-blanking input ($\overline{RBI}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (responsive condition).

Note 5: When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is OPEN or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

Functional Description

The DM74LS47 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{RBI}$ blanks the display and causes a multi-digit display. For example, by grounding the $\overline{RBI}$ of the highest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{RBI}$ of the lowest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e.: by driving $\overline{RBI}$ of a intermediate decoder from an OR gate whose inputs are $\overline{BI/RBO}$ of the next highest and lowest order decoders. $\overline{BI/RBO}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{RBO}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{BI/RBO}$ can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to $\overline{BI/RBO}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{LT}$ turns on all segment outputs, provided that $\overline{BI/RBO}$ is not forced LOW.