DESIGN AND CONSTRUCTION OF A TRAFFIC LIGHT CONTROLLER FOR T- JUNCTION MULTIPLE MOVEMENT: A CASE STUDY OF F.U.T MAIN CAMPUS JUNCTION.

BY

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CERTIFICATION

This is to certify that this project titled "THE TRAFFIC LIGHT CONTROLLER FOR A T- JUCTION CROSS – ROAD" was carried out by "JIMADA CHECHEKO" under the supervision of "ENGR. JONATHAN KOLO" and submitted to the Dept. of Electrical and Computer Engineering for the award of B. Eng. in Electrical and computer Eng , FUT, Minna.

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DECLARATION

I hereby deciare that this project was solely and wholly design and constructed by me under the supervision of Mr. J. Kolo of Electrical and computer Engineering department, Federal University of Technology Minna for line 2001/ 2002 academic session.

7/3/2002

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STUDENT SIGNATURE

DEDICATION

This project is dedicated to Almighty Allah: my late father Alhaji Jimada Kolo and my mother Hajiya Zainab Jimada Kolo and also mu lovely uncle Professor A.A Idrees who stood as my father for their outstanding construction in terms of encouragement, support both financially, morally and otherwise to ensure the completion od this project. And finally "may Almighty Allah bless and reward everybody. Amen.

ACKNOWLEDGEMENT

All praise is unto the Almighty Allah (SAW) for spacing my life throughout this period

Secondly, special thanks and gratitude to my parents, Late Alhaji Jimada Kolo and also lovely uncle professor A.A Idrees for their cash and kind contributions, those who imbibe the initiative that "Education is the bedrock for present and future individual achievememts and upliftment" hence work tooth and mails to provide me with qualitative education. Of course, the above fact cannot be achieved without financial and moral supports. Kudos to them!

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They also rendered and gave encouragement to go onto the research work, which finally works the project, a success.

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ABSTRACT

The essence of this project is to design and construct a traffic light controller for a T-Junction cross road.

It is in bid for achieving proper controls that traffic signs and signal conspicuous among the traffic signs and signals and it is the heart of this project.

The project uses sequential circuit and combinational circuit designs to achieve the proper sequencing and transistor drivers, which amplify the output of the sequential and combinational circuits to drive traffic lamps.

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1.0 INTRODUCTION

The importance of traffic control and traffic signals and signs cannot be over emphasised.

Traffic control devices include all signs, markings, and signals places on or adjacent to a street or highway by public agencies in order to regulate, warn or guide traffic. If traffic control devices are to be effective, they should

- Fulfill a need
- Command attention
- Convey a clear, simple meaning
- Command respect of drivers and pedestrians
- Be placed so as to give users time for proper response

The signal sequence of traffic signal in Great Britain is red, red and Amber, Shown together, green and then Amber.

Both the Amber, and the red and amber periods are standardized u law, but the green time and the red time may vary to suit the particular road condition. The signal sequence in Nigeria is red and Amber shown together, Green, Green and Amber shown together, Amber, and then Red. The Nigeria sequence is used in this project. The light colours and their meanings are shown below:

Red ⇒ stop

Amber ⇒ General warning

Green and Amber ⇒ warning to passing traffic to get to stop

Red and Amber ⇒ warning to waiting traffic to get ready to pass

The signal head, which holds the latterns for showing the various colours, is nowadays a one piece molding in black polypropyiene fitted with flexible blank plastic cowls. These moldings are replacing the metal heads, still to be seen in many places to provide a measure of safety in the avert of accidents and also to eliminate the need for painting. The heads are made to suit the various traffic requirements and can include indicate arrows, pedestrian light or other regulatory signs. A range of flexible bounds with a white border may be fitted to the signal head to make it more visible to the drivers. As a further aid low voltage tungsten halogen lamps are used with an optical system, which incorporate a reflector and lens. This arrangement gives a particular bright light, which is important in cities where drivers must be able to see traffic signals easily against a background of brightly and other distractions.

There are three types of traffic signal installation in common use

- Fixed time
- Vehicle actuated
- Computer controlled

In the fixed time signal, the red and green periods are set to predetermined internals and remain unchanged until reset. The movement of a vehicle over a detector coupled to an automatic controller provides a green period in vehicle-actuated signals. In computer-controlled signals, a computer is programmed to control the traffic.

In this project, the fixed time signal is used and the fixed times are

Red – 50 seconds

Green –25 seconds

Amber – 5 seconds

As a further aid to understanding the report, the first chapter throws some light on some necessary basic topics.

The second chapter deals with the design of regulation power supply, voltage regulator circuit and also rectifier circuits and chapter two further more deals with the tuner (pulse generator), counters transistor logic. Second chapter goes further to state how the design and analysis of traffic light controller for a T-junction. Third chapter goes to present how the construction and coupling is been made and how some measurements been carries out after the construction and how the results agree with the design aims. The traffic lamp used here is a 40w, 240v tungsten filament lamp. Lamps of higher voltage can be used by simply changing the transistor, amplifiers and the current sourcing transformer to designed bigger ones. The fixed fine for the light colours can also be changed by some resistive and capacitive alteration in the timer circuit.

1.1 LITERATURE REVIEW

In order to provide safe and efficient traffic flows, uniform standards have been developed for the use of all Public Street and high easy facilities in the U.S.

The recommended height for post-mounted signals, measured to the bottom of the housing, is 8 to 15 ft above the sidewalk. Median mounting must be 4.5 ft or more in height. Signals suspended over the roadway shall have minimum and maximum vertical clearances of 15 and 19 ft. they must be visible to approach 100 ft for an 85 percentile speed of 20mph to 700 ft for 60mph.

SIGNAL CONTROL

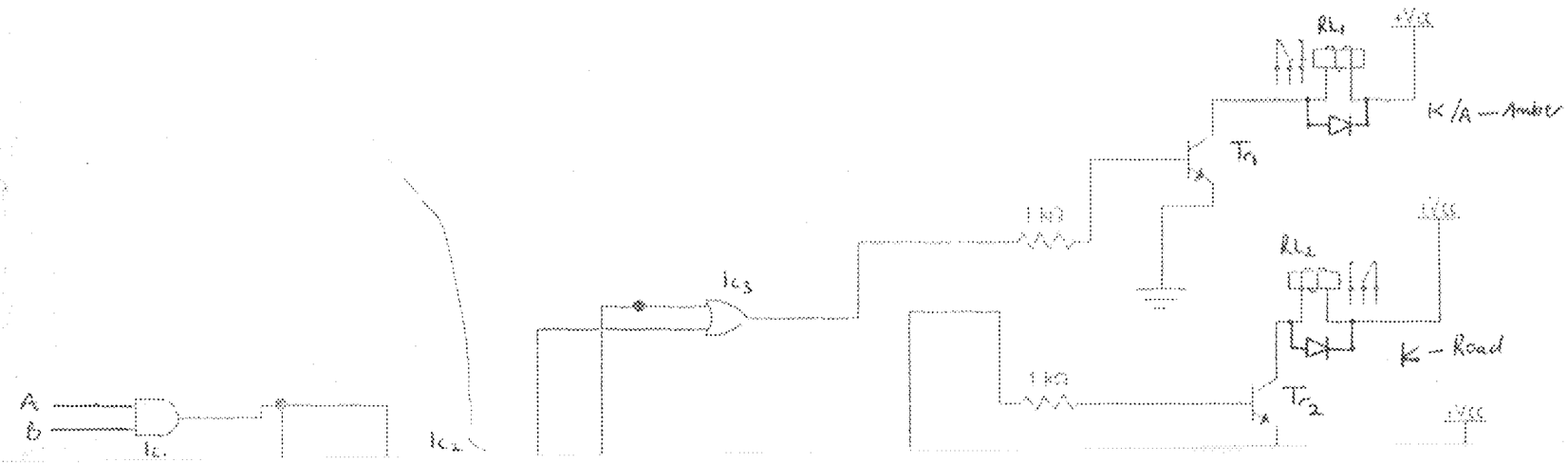
There are three types of traffic signal installation in common use: FIXED TIME, VEHICLE ACTUATES, and COMPUTER CONTROLLED.

In the fixed time signal, the red and green periods are set to predetermined intervals and remains unchanged until they are reset. Signals of this sort, therefore take no account of the time of day or night or of the traffic flow conditions.

With vehicle-actuated signals, it is the movement of a vehicle over a detector pad or detector loop couples to an automatic controller, which provides a green period so that it can proceed in safety. This reduces vehicle delay at the intersection by providing the most effective green and red times, and can eliminate signal changing altogether if there is no demand from any particular part of the intersection, and they can handle up to 12 independent traffic movements at an intersection.

These controllers are often linked together in groups of two or three for a limited system where several intersections are involved, or over a system where a large number of crossings and junctions occur on an approach road to a city. They can be adopted to fit into a computer controlled area system and then used for fixed time control in which the green and red times are set by the computer according to the time of day, the traffic density, and so on.

Area traffic control uses a computer in a traffic control office programmed for the storage of a number of traffic plane designed to match all the various traffic conditions likely to be encountered. The computer sends instructions to all various controllers in the area according to the particular plan selected. The


A
B
IC1
IC2
IC3
1 KΩ
1 KΩ
RL1
RL2
+VCC
+VCC
+VCC
K/A — Amber
K — Road
Tr1
Tr2

traffic control office can override the computer to introduce special priority routes emergency service vehicles or provide for unusual traffic flows.

VEHICLE DETECTORS

A vehicle- actuated traffic control system needs to have information about the flow of traffic through the intersection, and this information is supplies by detectors embedded in the road surface at the approach of the intersection.

Until recently these detectors were of the rubber pad variety, which consisted of pneumatic tubes placed across the traffic lane. As a vehicle passed over the detector, air in the tubes was displaced and the resulting increases in pressure operated or electrical contact, which passed a signal to the controller or computer. With today's traffic densities and the over increasing weight of road vehicles, the rubber pads rapidly become torn and useless. As a result of experiments undertaken to find a suitable replacement, it was the best. This sort of detector is buried in the road surface and cannot be damaged by vehicles. It is easy to install and is reliable.

Their inductive loop detectors can be seen as diamond or rectangular shapes in the road surface before the traffic signals. They consist of live loops connected to an oscillator so as to generate a magnetic field is disturbed and a signal pulse is passed to the controller or computer.

A close look at Nigeria traffic lights shows that Nigeria uses the fixed time signal. Analysis made on a typical traffic light signal in Minna, Niger State of Nigeria showed the following.

- The light colour changes from red; red and Amber; Green; Green and Amber; Amber, and back to red.
- Green takes 15 seconds, Red takes 1 minute, and Amber takes 3 seconds.
- The junctions with traffic light lane no roundabouts.
- For a cross junction, there are eight sets of traffic lights. Each set contains at least RAG lights. Some also contain a fourth arrows green light. Each traffic approaching the junction uses two sets of traffic lights that shows the same thing, are set towards the other set away from the traffic after the junction.

CHAPTER TWO

DESIGN OF REGULATED POWER SUPPLY

2.1 INTRODUCTION

The power supply is the most basic section of any electronic circuit. Practically all electronic systems require one or more power supplies, the simplest and most effective being a dry battery, while this has the advantages of being simple and having a low output impedance, it suffers from a limited useful life and poor long-term voltage stability.

The most common form of power supply comprises of a rectifier circuit, which provides a unidirectional but unstabilised output, followed by a filter circuit to smooth out ripples in the output voltage and current, and in some cases (as in this project) followed by a voltage regulator, which maintains the output voltages at a predetermined value despite variations in loading.

2.2.1 CHOICE OF RECTIFIER CIRCUIT

There are three available types of rectifier circuit compatible with single-phase a.c mains voltage. They are (1) single-phase half wave rectifier circuit.

It has the advantage of being simple, but conduction is only during a half cycle of the a.c signal and therefore it has the disadvantage of yielding a low d.c value of load current and voltage compares with the other two rectifier circuit. Ripple reduction is also relatively less affective here.

ii. Center-tap full-wave circuit. Here the rectifier conducts during the half-cycles of the a.c signal and has d.c voltage and current twice that of the half-

wave circuit. The drives have higher peak inverse voltages than either the half-wave circuit or the bridge circuit.

iii. The bridge rectifier circuit. This is chosen for this project since it requires no center tap transformer which is difficult to come by and costly too. Secondly, the repetitive peak inverse voltage is one half that in the center-top circuit. However, the disadvantage if this circuit is that it is not possible to simultaneously earth one side if the power supply and one side of the output, otherwise part of the bridge circuit will be short-circuited.

2.2.2 THE BRIDGE RECTIFIER CIRCUIT

The bridge rectifier circuit is shown in fig 2.1 (a). it has four drives, diagonally opposite pairs of which conduct simultaneously, so that when point A is positive with respect to point B drives D1 and D2 conduct, D3 and D4 being reverse biased.

Since the project require a d.c supply of 5v, a 240v/9v transformer was used. The power is the smoothened and regulated at 5v. The repetitive reverse maximum voltage rating of each diode should be at least four times the r.m.s value of supply voltage = 9v. 4 × 9v =36v. Hence, a diode with VRRM =36V shall suffice. The diode IN 4001 has VRRM as 50v and is used in the circuit.

2.2.3 SMOOTHING THE RECTIFIED A.C SUPPLY

The output voltage from a simplifier circuit consist of a direct potential (or current), with a super imposed alternation ripple component. The object of smoothing is to raise he average level of d.c voltage and to keep the percentage ripple below the maximum specified at full load. This is done by use of filter circuit.

There are four types of filter circuit available; capacitor filter circuit, inductor filter, chokes input filter and the II filter.

2.2.4 CHOICE OF FILTER CIRCUIT

The design of an inductor filter is often a compromise between the weight, inductance and resistance. An increase in inductance improves the performance of the filter, but it causes an increase in weight, resistance, and cost of the choke. Inductor filter produce very low output voltages when used with half- wave rectifier circuits. For these reasons, it is not chosen for this project.

In choke input filter, for low values of load current, the circuit tends to operate as a simple capacitor discharge periods and this brings about rapid reduction in terminal voltage with load current.

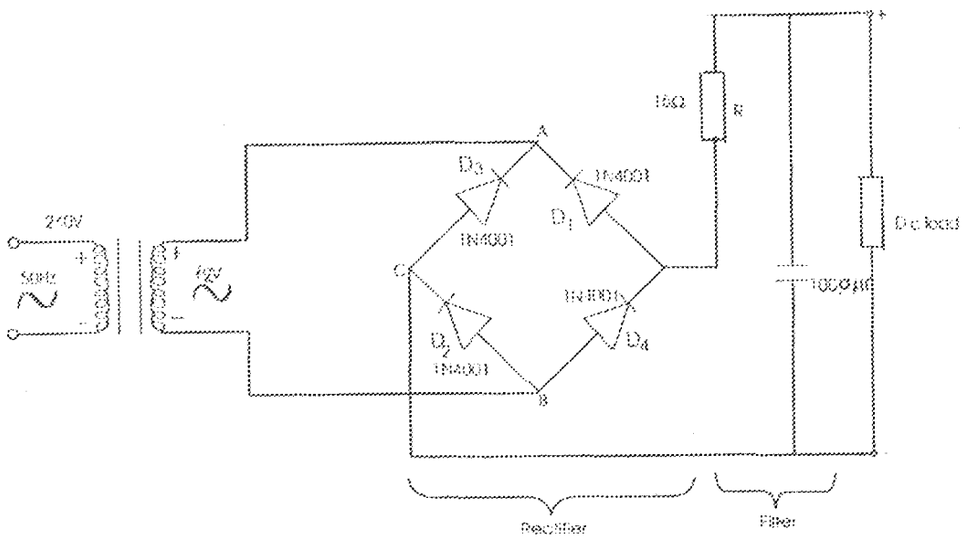
The capacitor filter circuit is the simplest form of harmonic filter circuit and is chosen for this project. It is not as costly as the inductor- based filter, and is not equally efficient. For best filtering, the reactance of the capacitor at the ripple frequency should be much lower than the resistance of the load. In this case the load presented to the rectifier is no longer completely resistive and a large proportion of the diode current flows into the capacitor.

The capacitor filter circuit is shown in fig 2.1a and the load voltage and current waveform associated with the circuit are shown in fig 2.1c.

Between t1 and t2 (Fig 2.1c) the supply potential is greater than the voltage across the capacitor, and current flows from the supply into the capacitor and load.

Between t2 and t3, the supply potential is lower than that on the capacitor, causing the D1 and D4 to be reverse biased. During this period, the capacitor discharges and maintains the load potential.

To reduce the ripple voltage to a low level, a large value of capacitance is used (1000MF electrolytic capacitor).



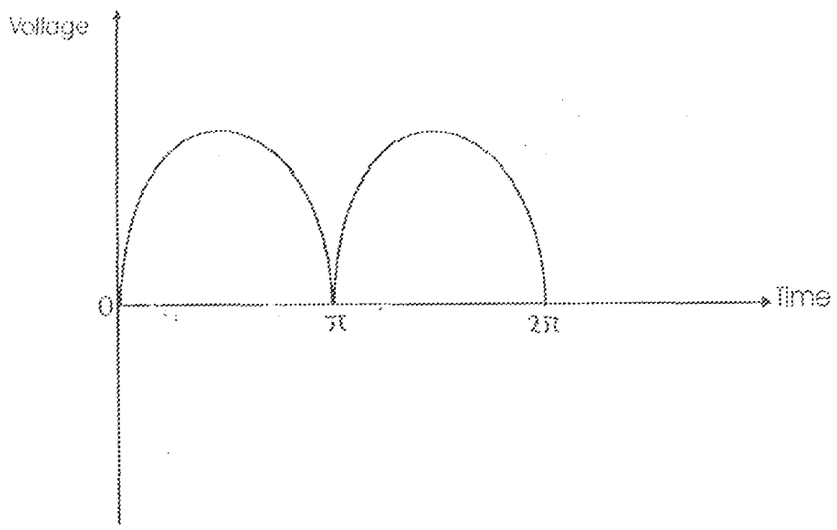


fig 2.0 full wave bridge rectifier, smoothened circuit and its waveform

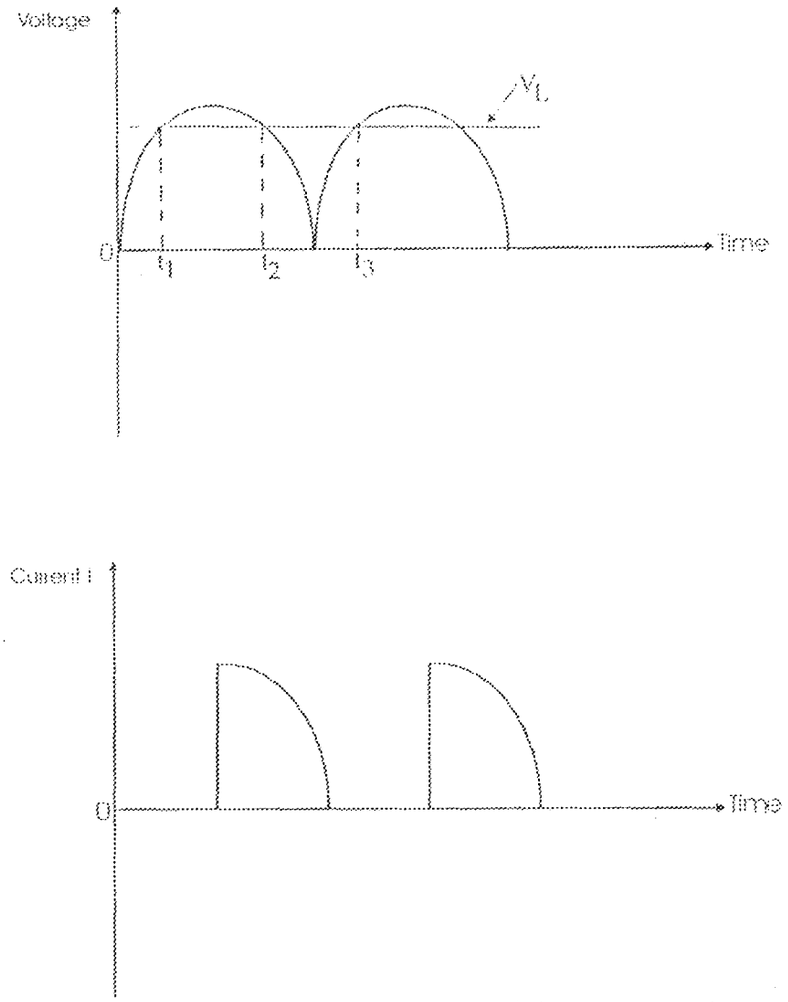


Fig 2.0 full wave bridge rectifier, smoothened circuit and waveforms

2.3.1 THE TIMER (PULSE GENERATOR)

The function of the timer is to generate timed pulses that are counted by the counter. In this project, the 555 Timer is used and is connected as an stable multivibrator is shown in fig 2.4.

When powered with +5v and ground, a 555 timer IC in the circuit of fig 2.4(a) will produced a continuous train of pulses, which are directly TTL and cmos compatible. The circuit operation is described as follows.

When power is applied, the output on Pin 3 is high. The timing capacitor from Pin 2 to ground is changed through RA and RB in series, until the voltage in the capacitor is equal to 2/3 Vcc. An internal comparator senses when the capacitor reaches this value, changes the previously high output to a low state and turns on a transistor which discharges the capacitor detects when the capacitor has discharged down to 1/3 Vcc, switches the output to start the change part of the cycle again.

Frequently of the output pulses can be determine from the formula.

$$F = \frac{1.44}{(RA + 2RB)\,C}$$

or from the chart in fig 2.4(b). To use the chart, select the frequency you want on the horizontal axis, follow this frequency line upward until it intersects on available capacitor value and then read the value for RA + 2RB from the nearest diagonal line.

For an approximately square wave output, RA should be much smaller than RB. The maximum RA + RB is 1 kilometer. Timing capacitors are always required from Vcc to ground and from Pin 6 to ground.

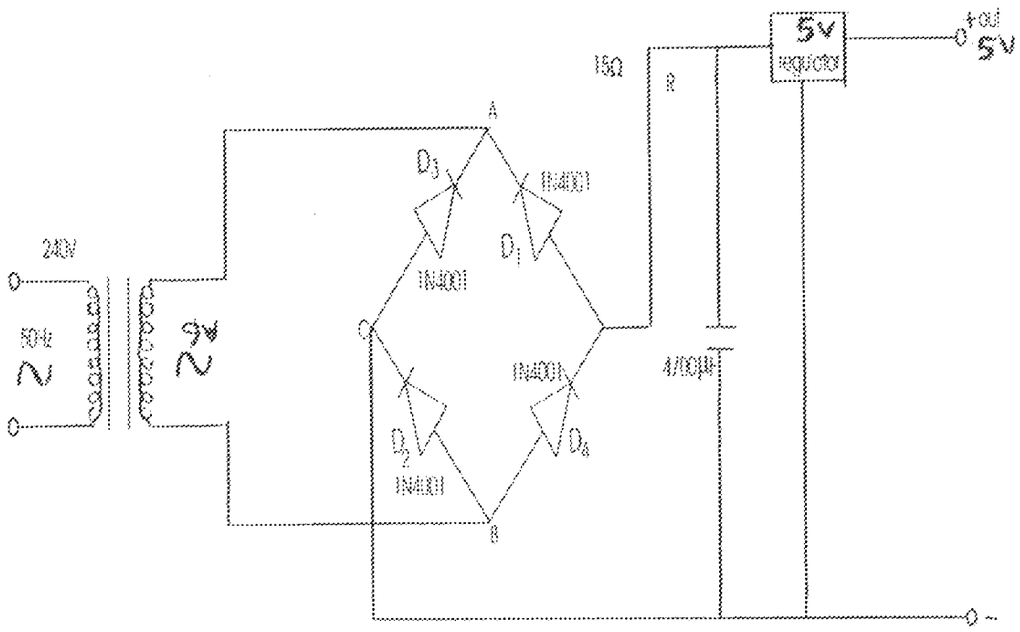


Fig 2.1 5V power supply

2.3.2 CALCULATION FOR C, RA AND RB

The total period for charge and discharge is

$T = t_1 + t_2$

$= 0.693 (Ra + 2Rb) \times C$ Second

So that output frequency is given as

$$F = \frac{1}{T} = \frac{1}{0.693 (Ra + 2Rb) \times C}$$

$$= \frac{1.44}{(Ra + 2Rb) \times C}$$

2.3.3 COMPONENTS AND VALUES

The value for C1 = 1000MF

The value for Ra = 1K

Therefore to calculate for Rb from the formula above

$$F = \frac{1.44}{(Ra + 2RB) \times C}$$

$$\Rightarrow T = \frac{1}{F}$$

$T = 0.693 (Ra + 2Rb) C_1$

$7 = 0.693 \times 1000 \times 10^{-6} (10^3 + 2Rb)$

$= 6.93 \times 10^{-4} (1 \times 10^3 \times 2 Rb)$

$= 0.693 + 1.386 \times 10^{-3} Rb$

$7 - 0.693 = 1.386 \times 10^{-3} Rb$

$$Rb = \frac{7 - 0.693}{1.386 \times 10^{-3}}$$

$= 4.55k$ 4.6K

Then the preferred value chosen is 4.7K.

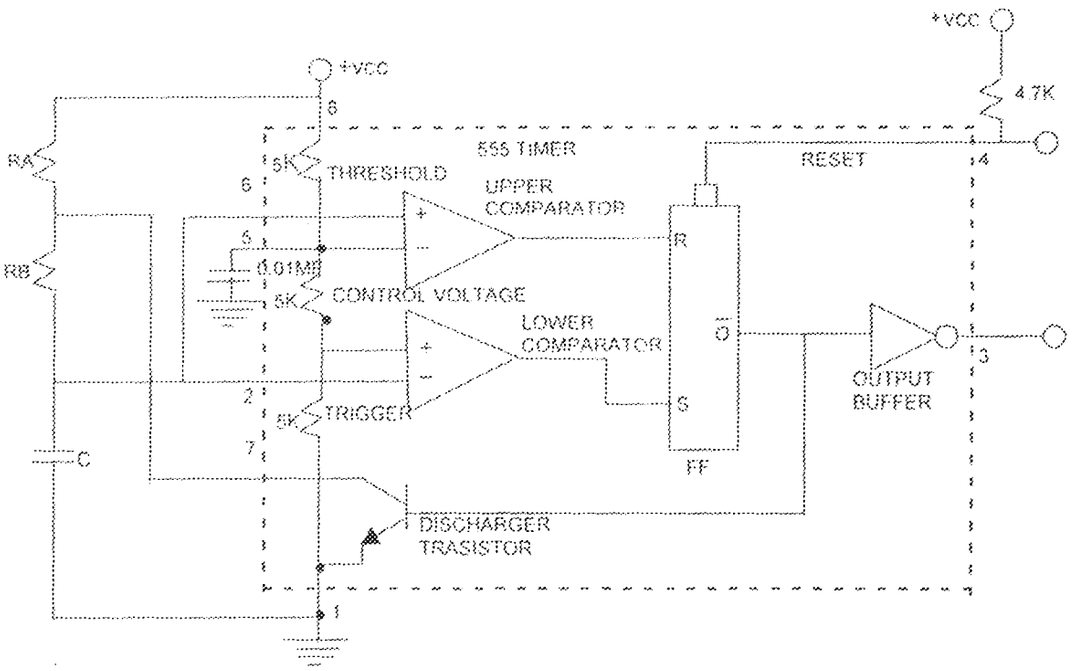


Fig 2.3 LM 555 TIMER IC USED AS A TTL OR CMOS PULSE SOURCE

Therefore a variable resistor of 10k was used to vary the needed value out of il. The value of resistors used for this design work are Rb = 4.7K. The value of c, is 1000MF.

These values of RA and RB are chosen not only because they satisfy the frequency formula but also they are available in the market.

2.4.1 COUNTERS

Counters are divided into two main groups. Asynchronous or ripple counter and synchronous counters.

The term 'ripple' indicates sequentially or ripples down through the chain of flip-flops. For a four stage binary counter made of four flip-flops, the output of the last flip-flop will not change until four flip-flop propagation delays after a negative edge of the input clock (for a trading edge triggered counter). This means that the counter is asynchronous because the outputs are not directly in synchronous with the clock.

The ratio of the input frequency to the output frequency to the output of a counter is called its 'modulo'. A single flip-flop is a module- 2 counter because input frequency is two times the output frequency. Ripple counters, however, eir disadvantages, which are treated later in this chapter.

synchronous counter is one in which all the outputs change at the same time because all the flip-flop are directly at the same time.

The trick with synchronous counter is that the output set up the j and k inputs. Then the next clock pulse will toggle or not toggle each flip-flop to the desired output state. This very powerful technique can be used to produce counter of any modulo or output count sequence.

An n-stage counter will have 2^n unique states. The least significant bit (LSB) of a counter is that bit changes most often. A counter that goes through n-states and then starts over again is called a modulo-n counter.

2.4.2 DISADVANTAGES OF RIPPLE COUNTER.

Although it is generally the least expensive of counters, the ripple of a ripple counter can give the designer cause for a trip to the aspirin bottle.

This counter is called a ripple counter because when the counter goes from iiii to 0000...(for 4-stage counter), the first stage causes the second to flip, the second causes the third to flip, the third the fourth and so on. In other words, the transitions of the first stage ripples through the stages are briefly entered.

For example, to go from IIII to oooo it must go through IIII state 15

III0 state 14

1100 state 12

1000 state 8

0000 state 0

If the designer has gate that will change during state 12, a brief spike will be seen at the gate output every time the counter goes from state 15 states to 0. This is also true when it goes from state 13 to 14; 1101, then 1100, and 1110.

The ripple counter is then a very inexpensive and a very dirty counter, in so far as unwanted spikes are concerned. The design procedures that follow synchronous counter overcome this serious limitation.

The second major problem of the ripple counter is the delay between the time at which the first flip-flop in a chain changes its. The counter is arranged in

TTL IC as SN 7493, which contains series connection of four stages complementing flip- flops. The output of each flip-flop is connected to the clock input of the next higher order flip-flop. Shown below in figure are the functional 4. Bit synchronous counter diagram with pin connections of the SN 7493.

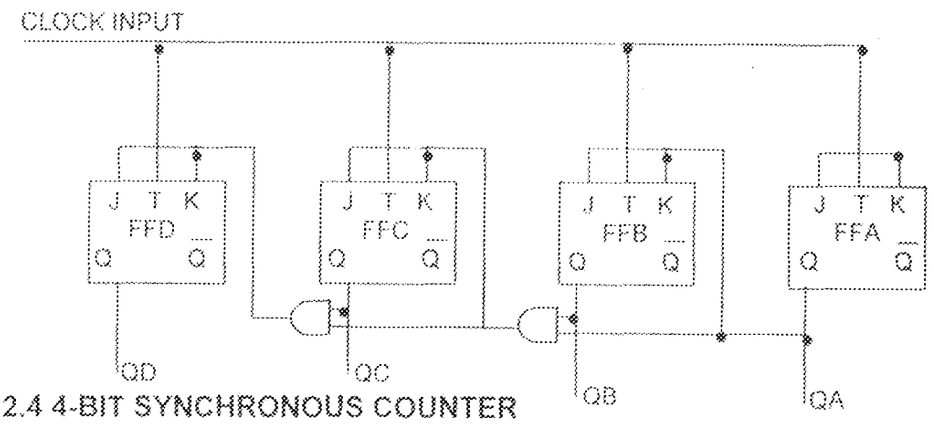


FIG 2.4 4-BIT SYNCHRONOUS COUNTER

The counting is sequentially, showing the decoding outputs with periods. The Rp(i) and Rp(2) inputs form direct clear. The Q outputs of SN 7493 are high as it is show by the reset/ count function table of .. 2.1. if the counter is to count correctly, at most one of the Rp inputs must be held low.

TABLE 2.1

RESET	INPUT	OUTPUT
Rp(1)	Rp(2)	QD QC QB QA
1	1	0 0 0 0
0	x	COUNT
X	0	COUNT

Reset/count function table

Note: 1=high level, 0=low level, X=don't care. The outputs of 4-bit synchronous counter are decoded using logic gates.

For the purpose of this project the outputs of the counter are decoded using the OR, AND and NOT gates. Before using these logic gates to implement the counter output, it is necessary to explain the truth table and the transition for all the four roads, K, L, M, and N.

TABLE 2.2

QC	QC	QB	QA	
0	0	0	0	
O	O	O	1	ROAD K
0	0	1	0	
0	0	1	1	← Y_K
0	1	0	0	
0	1	0	1	ROAD L
0	1	1	0	
0	1	1	1	← Y_L
1	0	0	0	ROAD M
1	0	0	1	
1	0	1	0	Y_M
1	1	0	0	←
1	1	0	0	ROAD N
1	1	0	1	
1	1	1	0	Y_N
1	1	1	1	←

Truth table for count output. Note Y indicates the amber transition.

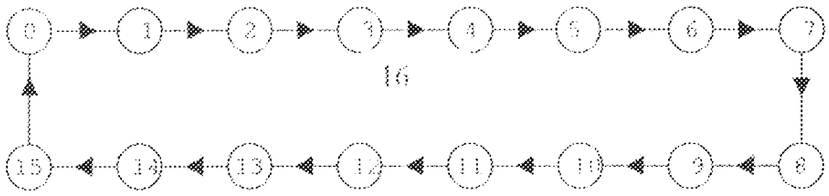


FIG 2.6 COUNTER STATE DIAGRAM

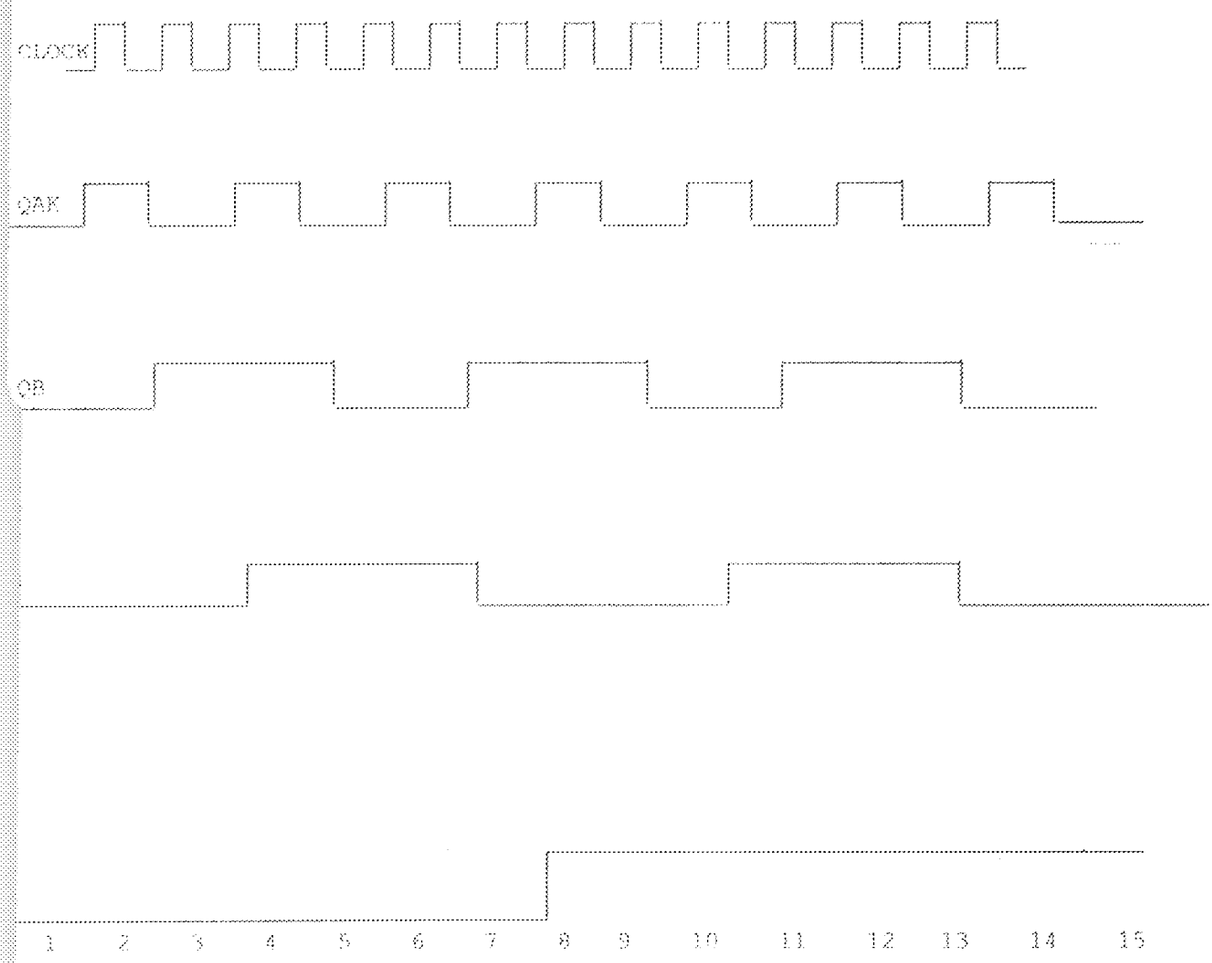


FIG. 2.7 COUNTER TIMING DIAGRAM

2.4.4 COMBINATION LOGIC AND BOOLEAN ALGEBRA

A combinational logic circuit is considered generally to possess a set of inputs; a memory less logic network to operates on the inputs and a set of outputs. The binary value of any output in a combinational logic circuit is determined solely by the present combination of binary input values and no dependence on prior input values. Further more, as long as the input values are maintained.

A Boolean function can be defined either by a truth table or by an algebra equation. A Karnaugh map is a graphical form of truth table consisting of square or rectangular array of adjacent cells. A Boolean function utilizing "n" variables requires a karnaugh map made up of 2^n cells. Each cell possesses a unique address, specified by the row and column in which the cell resides. The full address of any cell differs by no more than one digit from the address of any adjacent. Single numerical values of 'o' or '1' are entered in each cell. The karnaugh map is an effective way of reducing and simplifying Boolean functions.

Boolean expressions may be rearranged validly using Boolean algebra. Boolean algebra is used to manipulate and simplify Boolean expressions. The Boolean algebra properties are listed below X, Y, and Z are variables.

(1) X.O = O

(2) O.X = O Properties of the

(3) X.1 = X AND function

(4) 1.X = X

(5) $X+0 = X$ properties of the

(6) $0+X = X$ OR function

(7) $X+1 = 1$

(8) $1+X = 1$

(9) $X.X = X$ combining a variable with

(10) $X.\overline{X} = 0$ itself or its compliment

(11) $X+X = X$

(12) $X+\overline{X} = 1$

(13) $\overline{\overline{X}} = X$

(14) $XY = YX$ Double complementation

(15) $X+Y = Y+X$ Cumulative law

(16) $X(Y+Z) = XY+XZ$

(17) $X+YZ = (X+Y)(X+Z)$ Distributive law

(18) $X(YZ) = (XY)Z$ Associative law

(19) $X+(Y+Z) = (X+Y)+Z$

(20) $X+XY = X$

(21) $X(X+Y) = X$ Absorption

(22) $X+\bar{X}.Y = X+Y$

(23) $X(\overline{X+Y}) = XY$ An identity

(24) $\overline{X+Y} = \bar{X}.\bar{Y}$ Demorgan's law

(25) $\overline{X.Y} = \overline{Y+Y}\ \overline{\ }$

2.5.1 TRANSISTOR-TRANSISTOR LOGIC (TTL) PROPERTIES

Vcc is the power supply voltage requires operating the entire device or IC. Input and output voltages are the logic level signals for each gate on the device. The absolute maximum Vcc of TTL device is 7v. Any voltage beyond this damages the devices. The 5400 series have maximum operating voltage 5.5v and a minimum of 4.5v, while the 7400 services have maximum and minimum operating voltage of 5.25v and 4.75v respectively.

The TTL gate has a minimum logic 1 input of 2v and a maximum logic 0 input voltage of 0.8v. On the output of the gate, it has minimum logic 1 output voltage of 2.4v and a maximum logic 0 output high voltage is higher than the minimum voltage required for an input high on a following gate. This 0.4v difference is referred to as a noise margin. It ensure that a small noise transistor on a connecting line cannot change the state of the rest gate.

A gate output is said to sink current if it creates a current path from the input of a following gate to ground or to a negative supply. The maximum logic 0 input current for TTL gate is –1.6 mA. A minus sign on a current indicates that conventional current is flowing out of the indicated device pin. A plus sign on a current indicates that conventional current id flowing into that device pin.

The maximum logic 1 input current for a TTL gate is 40 microamperes. The fan-out is the maximum number of gate inputs that can be connected to a single gate output without preventing the output from reaching legal high and legal low voltage levels. Fan-out is equal to output gate current divided by input gate current. The fan-out for a standard TTL gate is 10.

The propagation delay is the tine needed for a change on the input of a device to cause a change in the output. The propagation delay of a TTL gate ranges from 10 to 25ns.

A TTL input left open acts as a high because there is no base- emitter current path through it. In practice, unused TTL AND or NAND gate inputs should be tied to Vcc with a 1-kilo ohm resistor. The 1 kilo ohm resistor protects the gate input from any large voltage spikes on the Vcc line. Unused OR or Nor gate inputs can be tied directly to ground.

Standard TTL outputs should not be connected together to avoid the fatal fight that may occur if one outputs tries to go high while the other tries to go low.

Bypass capacitors, typically 0.01 to 0.1 microfarad should be connected between Vcc and ground to filter out Vcc transient caused by gate switching states.

Connecting lead should not be greater than 12 to 14 in (30.5 to 35.6cm) for standard TTL.

2.5.2 DESIGN OF MODULO-16 SYNCHRONOUS COUNTER USING J-K FLIP-FLOPS (TYPE J-K DESIGN)

Due to the impending problems encountered with ripple counter as enumerated in chapter 1, synchronous counters has been chosen for this project.

In counter design, the first thing to do is to construct the basic transition table for the type of flip-flop to be used.

The type J-K flip-flop is a combination of type D and T flip-flops. The J and K leads control the mode in which the device operates. With both the J and K O's the flip-flop will remain unchanged upon receipt of the next clock pulse; the information remains unattered. With one state upon receipt of the device will go to the zero state upon receipt of the next clock pulse will cause the device to flip to the opposite state in typical T- fashion.

This operation is summarized in table.

The J-K flip-flop can be connected as type D or type T. this is why it is called a universal flip-flop.

Table 2.4

Operations of J-K flip flop

J	K	Response
0	0	unchanged
0	1	0
1	0	1
1	1	flip

The basic transition table for J-K flip-flop is shown in table.

Table 2.5 Transition table for J-K flip-flop

Q(t)	Q(tt1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Where X = don't care condition

Q(t) = state of flip-flop before clock pulse is received.

Q(tt1) = state of flip-flop after transition.

The state diagram for the modulo 16 counter is shown in fig and the counter state table is shown in table.

Table 2.6

Present state	Next state							
D C B A	D C B A	JD	KD	JC	KC	JB	KB	JA	KA
0 0 0 0	0 0 0 1	0	x	0	x	0	x	1	x
0 0 0 1	0 0 1 0	0	x	0	x	1	x	x	1
0 0 1 0	0 0 1 1	0	x	0	x	x	0	1	x
0 0 1 1	0 1 0 0	0	x	1	x	x	1	x	1
0 1 0 0	0 1 0 1	0	x	x	0	0	x	1	x
0 1 0 1	0 1 1 0	0	x	x	0	1	x	x	1
0 1 1 0	0 1 1 1	0	x	x	0	x	0	1	x
0 1 1 1	1 0 0 0	1	x	x	1	x	1	x	1
1 0 0 0	1 0 0 1	x	0	0	x	0	x	1	x
1 0 0 1	1 0 1 0	x	0	0	x	1	x	x	1
1 0 1 0	1 0 1 1	x	0	0	x	x	0	1	x
1 0 1 1	1 1 0 0	x	0	1	x	x	1	x	1
1 1 0 0	1 1 0 1	x	0	x	0	0	x	1	x
1 1 0 1	1 1 1 0	x	0	x	0	1	x	x	1
1 1 1 0	1 1 1 1	x	0	x	0	x	0	1	x
1 1 1 1	0 0 0 0	x	1	x	1	x	1	x	1

From the above table 2.2 using karnaugh maps to simplify the logic give a group of table-designated table 2.6

2.6.1 THE OUTPUT STAGE

For this project, the output stage is made up of transistor amplifiers, switching diodes, relays and indicator lamps.

When the output of the logic circuit is high, about 4 volts, the transistor, T, is driven into saturation and begins to conduct. At this time the collector voltage is approximately zero, so that all the 12 volts connected to the relay will appear across the relay coil. With this coil becomes energized and this consequently closed, thus closing the ac path through the lamp then turns ON. This lamp remains ON for as long as the logic output is on the high state. On the other hand, when the output of the logic circuit turns zero, the transistor will be cut-off, and the collector voltage will be high (approximately 12 volts). As a result of this, the coil of the relay is de-energies and this bring the contacts to be open. Then the lamp goes off. This explanation is for the normally open contacts, which is used in this project for the control of the green lamps. These operations occur in single relay called the single pole double throw relay at the same time.

Furthermore, another relay circuit: a single pole- single throw normally open contact is used for the amber lamps. In this, the explanation for the single pole-double throw normally open contacts holds. The relay is used for the control of the green and red lamps and that used for the control of the amber lamps, a diode, D is used and this serves to protect the transistor from eddy current from the relay coil at switch off. The component value of the resistor used in the base circuit was calculated as shown below. The loop current equation emitter of the transistor.

If VR = Relay voltage = 12 volts

RL = Relay resistance = 420 ohm

IC = Collector current

Ib = Base current

Hfe = Current gain = 150

Vce = Collector to emitter voltage

Vce(sat) = Saturation-collector to emitter

(For an N.P.N silicon transistor at sat Vce 0.3)

Then we can write

$V_R = R_L IC + Vce\ (sat)$

$R_L Ic = V_R - Vce\ (sat)$

$$IC = \frac{V_R - Vce\ (sat)}{R_L}$$

$$= \frac{12 - 0.3}{420}$$

27.9mA

But hfe – Ic/Ib

Then Ib = Ic/hfe

$$Ib = \frac{27.9\times10^{-3}}{150}$$

$$= 185.7mA$$

By taken KVL between base and emitter loop we have:

Vb = IbRb + Vbe (sat)

Where Vb = Base voltage = 4.5 volts

Ib = Base current = 185.7 mA

Vbe = Base emitter voltage

Vbe(sat) = Saturation-Base to Emitter (for an N.P.N silicon transistor at sat Vbe = 0.7)

Hence from equation we can deduce that:

$$Rb = \frac{Vb-Vbe(sat)}{Ib}$$

$$=\frac{4.5 - 0.7}{185.7\times10^{-6}}$$

= 20.5kiloohm

2.6.2 COMPONENTS AND VALUES

Diode D=IN 4148

Relay coil resistance RL =420ohm

Transistor T = Bc 107 (NPN)

Base resistance Rb = 22k

Base voltage Vb = 4.5 volts

Vbe(sat) = 0.7 volts

Base current, Ib = 185.7mA

Collector current, Ic = 27.9mA

Vce (sat) =0.3 volts

Relay voltage, VR =12 volts

Current gain, hfe =150.

It is very important to state the types of logic gates use in this project.

i. The Boolean expression: A+B =Y; where sign + denote OR

The logic symbol:

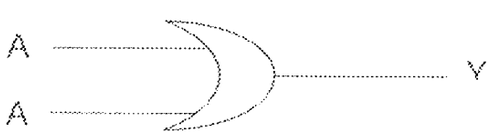


Fig. 2.7

The truth table for an OR gate Table 2.7

B	A	Y
0	0	0
0	1	1
1	O	1
1	1	1

ii. The Boolean expression: $Y=A$ or $A=Y$

The logic symbol: for inverter

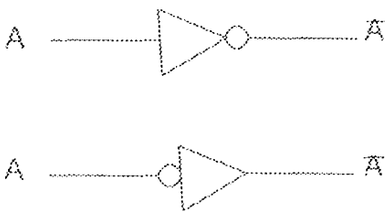


Fig 2.8

The truth table for an inverter Table 2.8

A	Y
0	1
1	0

Output state and the time at which a later stage changes its output state. This time delay yields in the output count.

Due to the above defects of the ripple counter, the synchronous counter is used in this project. And the outputs are as described in the function table of table 2.0

Table 3.1

		Road K	Road L	Road M	Road M^1	Road N	Pulse Period(second)
STATE	D C B A	R A G	R A G	R A G	R A G	R A G	
0	0 0 0 0	0 0 1	1 0 0	1 0 0	0 0 1	0 0 1	7 sec.
1	0 0 0 1	0 0 1	1 0 0	1 0 0	0 0 1	0 0 1	7 sec
2	0 0 1 0	0 0 1	1 0 0	1 0 0	0 0 1	0 0 1	7 sec
3	0 0 1 1	0 0 1	1 0 0	1 0 0	0 1 1	0 1 1	7 sec
4	0 1 0 0	0 0 1	1 0 1	1 0 0	1 0 0	1 0 0	7 sec
5	0 1 0 1	0 0 1	0 0 1	1 0 0	1 0 0	1 0 0	7 sec
6	0 1 1 0	0 0 1	0 0 1	1 0 0	1 0 0	1 0 0	7 sec
7	0 1 1 1	0 1 1	0 1 1	1 1 0	1 1 0	1 0 0	7 sec
8	1 0 0 0	1 0 0	1 0 0	0 0 1	0 0 1	1 0 0	7 sec
9	1 0 0 1	1 0 0	1 0 0	0 0 1	0 0 1	1 0 0	7 sec
10	1 0 1 0	1 0 0	1 0 0	0 0 1	0 0 1	1 0 0	7 sec
11	1 0 1 1	1 1 0	1 0 0	0 1 1	0 0 1	1 1 0	7 sec
12	1 1 0 0	0 0 1	1 0 0	1 0 0	0 0 1	0 0 1	7 sec
13	1 1 0 1	0 0 1	1 0 0	1 0 0	0 0 1	0 0 1	7 sec
14	1 1 1 0	0 0 1	1 0 0	1 0 0	0 0 1	0 0 1	7 sec
15	1 1 1 1	0 0 1	1 0 0	1 0 0	0 0 1	0 0 1	7 sec

(iii) The Boolean expression: A . B =Y

The logic symbol: for an AND gate

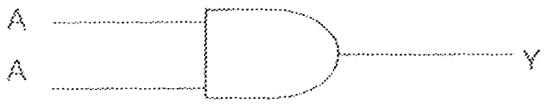


Fig 2.9

The truth table: for an AND gate Table 2.9

B	A	Y
0	0	0
0	1	0
1	O	0
1	1	1

And other logic gate include the non-inverting buffer/ driver, the NAND gate and NOR gate which are obtained by combining the NOT gate with the AND and OR gates respectively. Furthermore there are the exclusive OR and exclusive NOR gates with symbols XOR and XNOR respectively.

2.6.2COMPONENTS AND VALUES

The NOT gate = ECG 7405

The AND gate = ECG 7408

The pulse generator = 555 timer

The OR gate = ECG 7432

The counter = SN 7493

2.7.1 THE TRAFFIC LAMP

The lamp chosen for this project is a 240v. 40w lamp

Power = current x voltage i.e P = I V

i.e I = P/v = 60/240 = 2.5 = 250 mA

A typical IC output current cannot drive the 60w lamp. Therefore, an amplifier is needed to amplify the IC output current to such a level that can drive the lamp. In this project, transistors are used to amplify the IC output current.

A suitable transistor will be able to pass safely 250 mA of current between the collector and emitter. Since the IC output is a positive voltage, the transistor will be such that a positive voltage biases it. Hence, an NPN transistor is ideal. The transistor has to have an appreciable life so as to be able to raise the collector current to such as amount that can drive the lamp. The transistor BEY 51, which is a low level power transistor with gain of 30 at 150mA collector current. It has an average maximum collector current of 1000mA. The lamp and transistor connection is also shown in fig. 3.2. The transistor is connected in common emitter configuration and it is operated are the safest regions to operate with least power dissipation.

3.1 CONSTRUCTIONS AND COUPLING:

3.2 CONSTRUCTION:

The complete circuit for the system was first built and wired on project board. After discovered that the relay contacts were behaving as expected on the board, the vero-board. Ic sockets was first inserted into strategic position on the board and then soldered. Other components are also carefully soldered on the board. Finally the Ics were then places into the IC sockets.

It is important to state here that before soidering the component and boards were thinned so as to avoid the over- heating of the board and also to avoid dry joints.

3.3 COMPONENTS AND TESTING

The circuits were couples together to make up the complete traffic controller system for the T-Junction. The signal indicator were made up of three colours of lamps for each signal heads for the roads. This signal heads always consist of the red the green lamps on top, amber in the middle and green light comes at the bottom.

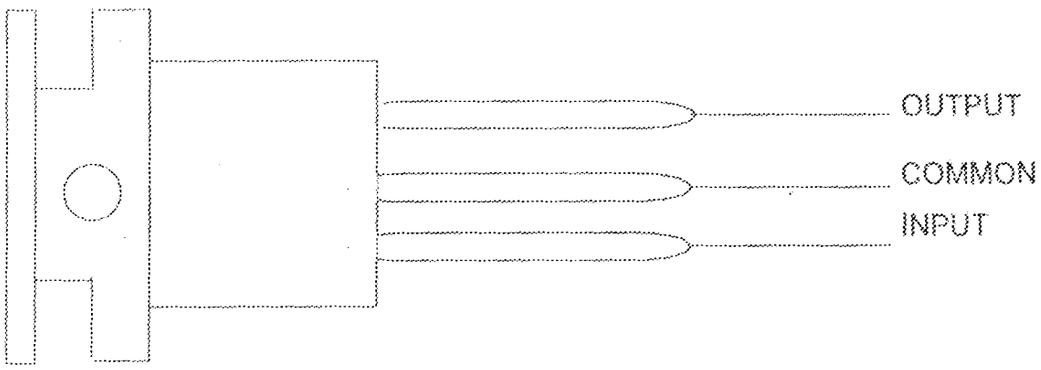


Fig 3.1 AN 7805 CT VOLTAGE REGULATO

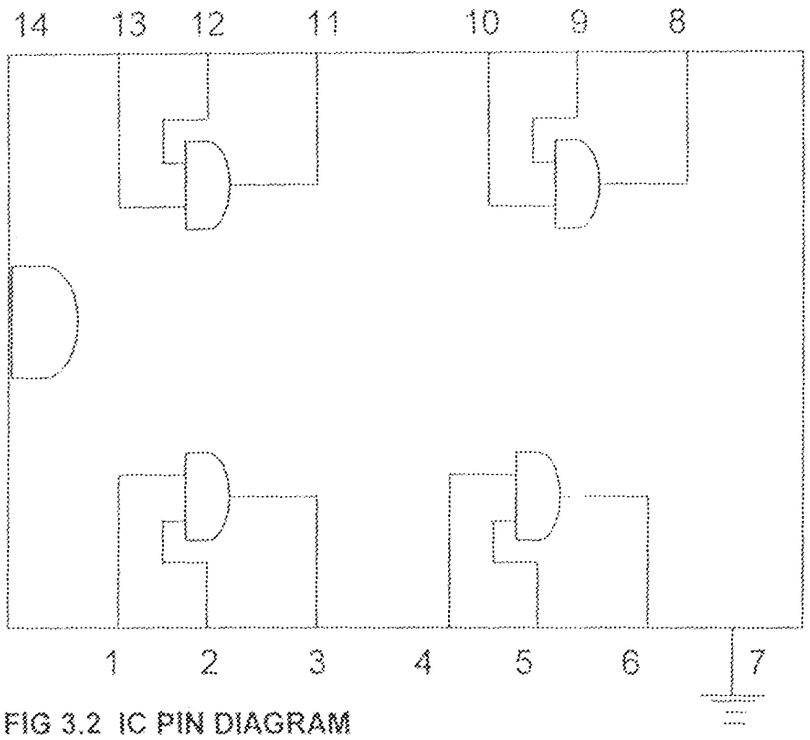


FIG 3.2 IC PIN DIAGRAM

The design is such that some roads consist of more than one green lamp with arrow indicating the direction of movement for vehicles it is intended to control. Furthermore, the bulbs rated 40 watts each were connected to the main supply with relay contacts as switches. It was ensured that the coupling was one properly and the over- all circuit was tested and found working.

The over all circuit design is enclosed in this project book

TABLE 3.2.1 BOOLEAN EXPRESS FOR TRAFFIC LIGHT

- Period 1, Roads N, M^1 and K = 1 which means road are to move (no interception).
- Period 2, Roads K, L= 1, the roads are free to move without any interception.
- Period 3, Roads M, M^1 = 1, the roads are free to move.
- Period 4, Roads M^1 , N are k = 1, the roads are free to move without no interception.

For the whole roads movement, the periods combination involved and also the simplification is done according to the output sequence using combinational logic and Boolean expression which is shown below.

❋Period 1 for Roads K, M^1 and N

$\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D}$

$\bar{B}\bar{C}\bar{D}(\bar{A} + A) + B\bar{C}\bar{D}(\bar{A} + A)$

$= \bar{B}\bar{C}\bar{D} + B\bar{C}\bar{D}$

$= \bar{A} + A = 1$

$\bar{C}\bar{D}(\bar{B} + B)$

$= \bar{C}\bar{D}$

$= \bar{B} + B = 1$

❋Period 2 for Roads K and L

$\bar{A}\bar{B}CD + A\bar{B}CD + \bar{A}BCD + ABCD$

$\bar{B}CD(\bar{A} + A) + BCD(\bar{A} + A)$

$\bar{B}CD + BCD$

$= \bar{A} + A = 1$

$CD(\bar{B} + B)$

$\bar{C}D$

●Period 3 for Roads M and M^1

$\bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D}$

$\bar{B}\bar{C}\bar{D}(\bar{A} + A) + B\bar{C}\bar{D}(\bar{A} + A)$

$\bar{B}\bar{C}\bar{D} + B\bar{C}\bar{D}$

$= \bar{C}\bar{D}(\bar{B} + B)$

$\bar{C}\bar{D}$

$= \bar{B} + B = 1$

●Period 4 for Roads K, N and M^1

$\bar{A}\bar{B}CD + A\bar{B}CD + \bar{A}BCD + ABCD$

$\bar{B}CD\ (\bar{A} + A) + BCD(\bar{A} + A)$

$BCD + BCD$

$= \bar{A} + A = 1$

$CD(\bar{B} + B)$

$= CD$

$= \bar{B} + B = 1$

Though this is done for Road Green and Red lamps . The combination of period for Amber lamps are done to allowed smooth transition and warning for movement without any problem.

The combination of periods for Amber lamps are as shown below.

Periods of Ambers

Period 1 = $AB\bar{C}\bar{D}$

Period 2 = $ABC\bar{D}$

Period 3 = $AB\bar{C}D$

Period 4 = ABCD

For the Amber to come ON, the periods combination involved according to table 2.3 and thew simplification using combinational logic and Boolean expression.

For Amber K = period 2 + period 3

$AB\bar{C}\bar{D} + A\bar{B}\bar{C}D$

$= AB(C\bar{D} + \bar{C}D)$

For Amber L = period 1 + period 2

$A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D}$

$A\bar{B}\bar{D}(\bar{C} + C)$

$= A\bar{B}\bar{D}$

For Amber M = period 2 + period 3

$AB\bar{C}\bar{D} + A\bar{B}\bar{C}D$

$= AB(C\bar{D} + \bar{C}D)$

For Amber M^1 = period 1 + period 2

$A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D}$

$A\bar{B}\bar{D}(\bar{C} + C)$

$= A\bar{B}\bar{D}$

For Amber N = period 1 + period 3

$A\bar{B}\bar{C}\bar{D} + AB\bar{C}D$

$A\bar{C}(\bar{D} + D)$

$A\bar{B}\bar{C}$

From the illustration above on the movements of the roads the fig 2.3 below shown transition sequence and the complete road structure at the junction and their movement

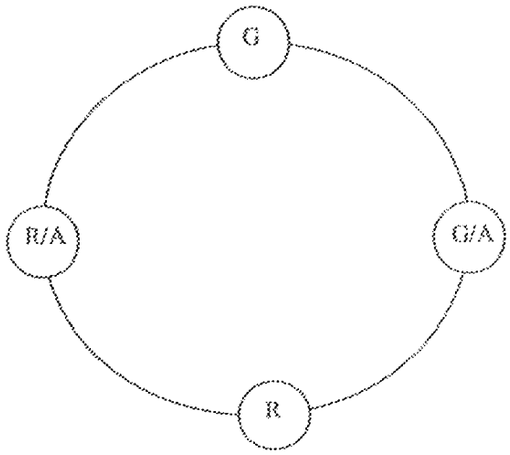
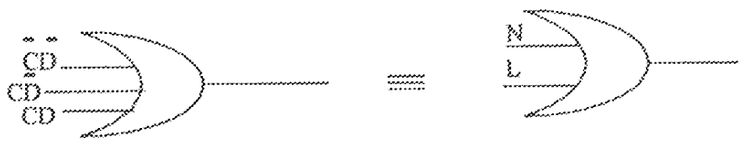


Fig 3.3: Transition of lamps for movements

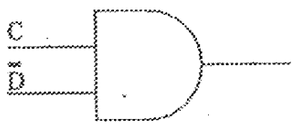
Then the combination of periods simplification for Roads movement is expressed below

For Roads movement is expressed below

For Road K = $\bar{C}\bar{D} + C\bar{D} + CD$



For Road L = $C\bar{D}$



For Road M = $\bar{C}D$

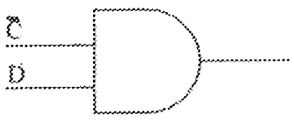
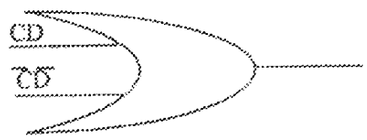


Fig 3.3

For Road $N = CD + \bar{C}\bar{D}$



For $M^1 = CD + \bar{C}\bar{D} + \bar{C}D$

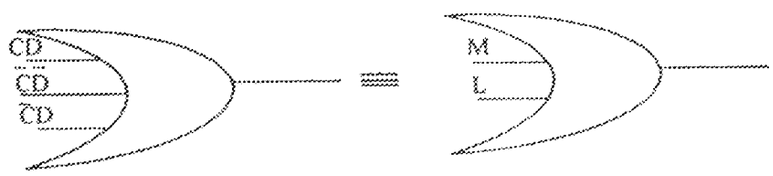


Fig 3.3

3.4 SUMMARY OF OPERATION:

Before I proceeded to the next chapter of this project, it is necessary to briefly explain the mode of operation of this traffic controller. 5 and 12 volts d.c were regulated from 240/9volts and 240/15volts transformers which were powered to the ac mains supply. The 5 volts supply provides the source required for the pulse generator and at the same time serves as the d.c source to the logic gates. On the other hands the 12 volts supplies the relay switch.

The pulse generator provides clock pulses, which is used to trigger the counter. Consequently the output of this counter were then decoded using the logic gates (AND), OR and NOT gates). The design was such that the output of these logic gates were used to operate the relay which were amplified by the transistor since the output of the logic gates were low. Depending in the states of this relays, the lamps were turn up or closes as the case may be. The full explanation of this had been explained.

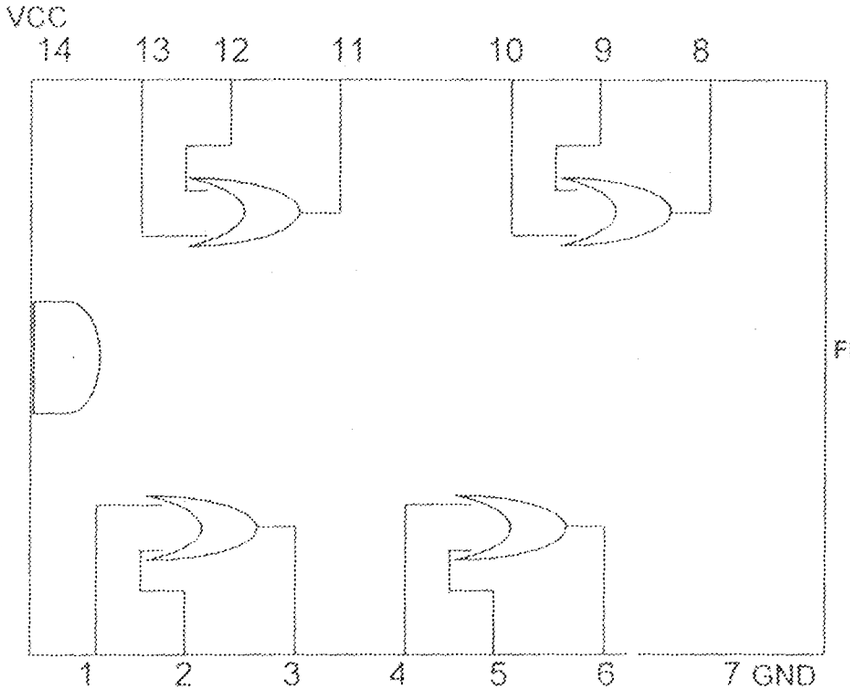


FIG 3.4 SN 7432 PIN DIA(

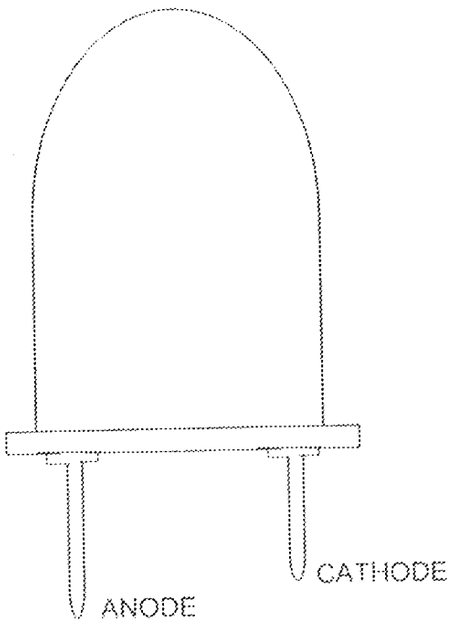


FIG 3.5 LED DIAGRAM

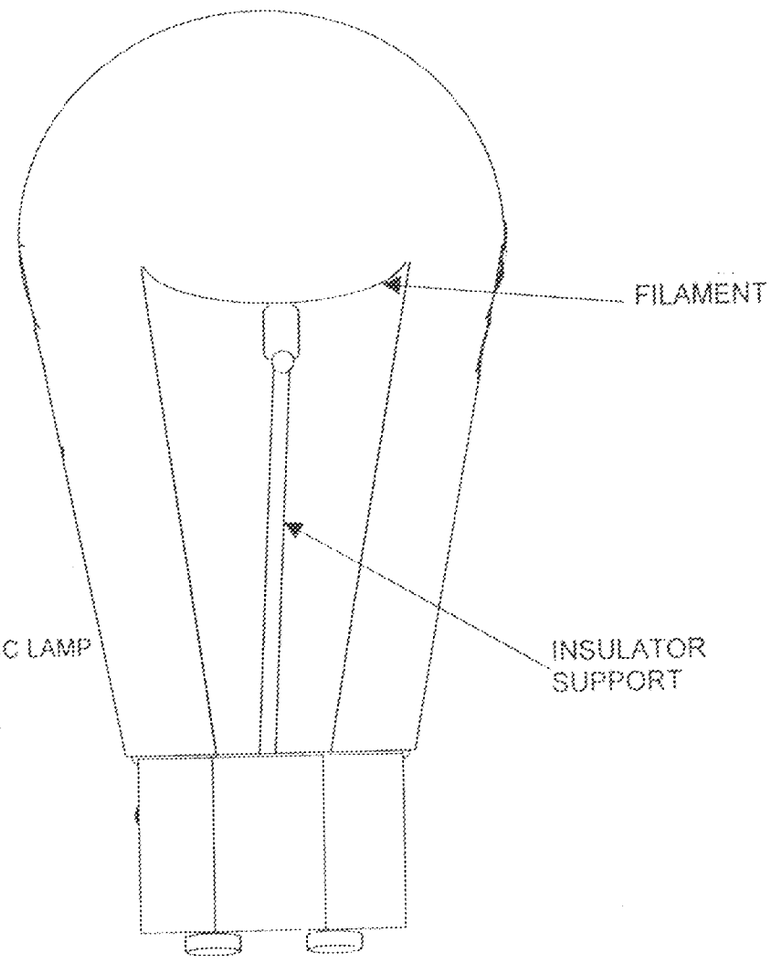


Fig 3.6 240, 40w TRAFFIC LAMP

CHAPTER FOUR

4.1 RESULTS AND CONCLUSION

4.2 RESULT/ DISCUSSION OF RESULTS

We have successfully been able to use the pulse generator to produce clock pulse whose periods depends on the duration desired. Table of this project shows the sequence and period for each of the lamps. From this table we observe that each state represents a clock pulse and the combinations of these pulses are used in the operation of the different time lengths of the lamps.

Furthermore, a brief analysis of this table shows that for road k, when the GREEN lamp comes up, other roads indicate RED. At the last state of this stage the AMBER of both road k and L comes up. This is an indication that both sequences should get ready for change. The movement now switch to road L, thereby making other roads to stop. Also at the last state, the AMBER of roads L and M comes up. It also important to state here that for the AMBER lamps to come up, say for that of road k, it is either state 3 OR 15. This has been indicated by enclosing all the AMBER lamps ON in the broken circle for simplicity.

Lastly, shown below are the lights changing sequence and the placements of these controllers on the roads. However, this changing sequence has been done based on this project design. Also, these signal head is just on attempt on how they can be place in the road.

3.5 THE RELAY

Relay is an electromechanical device, or solid state device operated by vary input, which in terms is used to control other devices connecied to its input. The movement of this mechanical part contact thereby the states of the contacts changes at switch on.

The relay used is a single pole double throw type which means it has a normally closed and normally open contact for both Green and Red lamps control. But for the Amber lamp a single pole single throw contact relay was used. It has only one normally opened contact and it used to control the number lamp at stipulate period.

The type of relay used are 12 volts, with 420 ohms resistance from the coil. This means that the expected current of the coil is about 28 mA, which serve as collector current. The relay coil resistance serves as collector resistance.

4.2.1 PROBLEMS ECOUNTERED

The major problems encountered during the cause of this project was in trying to combine the GREEN lamps for some roads. Another problem is in getting the placements for the signal heads. One has to go to the road safety office where we were directed to the police stations in the school vicinity. I have to state here that the police encountered were either ignorant of the information we needed or they refused to cooperate. Also what mentioning were some Ics bought as a new product but refuse to operate as expected.

4.2.2 RECOMMENDATION

Since using memory circuit miniaturized the system and is more reliable. The method or approach should be adopted for our traffic light controllers.

The increase in reliability help to solve the problem of break down of the system few months immediately after installation hence is preferable. Using combinational logic circuit components employs a lot interconnection, which definitely pose problem during fault finding. Tracing of fault becomes difficult. But as using memory chips reduces interconnections, definitely the problem of faultfinding will also be reduced.

4.3 CONCLUSION

It has been seen that traffic light controller can be design and constructed from the basis principles if electric counting and sequencing using simple logic gates.

To some great extent, the objectives of the design were achieved in the construction.

The duration of the RED, GREEN and AMBER lights can be either increase or decrease by altering the time of the timer circuit. Finance was one of the major factors that affected the type of materials used in this project. However, it could be recommended that to mount the traffic light on the T-junction, some improvements are necessary. First, the metal stand should be very strong and durable type.

4.4 REFERENCES

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