DESIGN AND CONSTRUCTION OF A CMOS (DIGITAL) LABORATORY KIT

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DEDICATION

To Iya, Gede, Mamma and my brothers and sisters

DECLARATION

This is to certify that this project design and construction of a CMOS (digital) laboratory kit was carried out by Bala Umar Shamsuddeen (2000/9812EE) under the supervision of Mr. A. Shehu for the award of bachelor of engineering (B. Eng) degree in electrical/computer engineering Federal University of Technology, Minna, Niger state.

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Chapter One
Introduction

1.1 Expository Introduction

The CMOS (Complementary metal oxide semi conductor) Laboratory kit as the name implies, is a laboratory equipment used for conducting experiments to investigate and demonstrate the functions and operations of CMOS integrated circuit (IC).

Thus, the CMOS laboratory kit could be taken as any other regular laboratory equipment, just like the oscillators, voltmeters, bread-boards etc., in that they have basically the same functions viz: used for conducting experiments.

However, the CMOS laboratory kit is a special laboratory equipment because it is designed to carry out different laboratory experiments without any peripheral connections. This is possible due to the fact that the CMOS laboratory kit contains a lot of different components and connections necessary to accommodate the different experiments. Furthermore, the CMOS laboratory kit is flexible in the sense that it can accommodate new components in order to enable new experiments which were not planned for originally.

Summarily, the CMOS laboratory kit functions in the following way. The kit already contains the components and the connections necessary for the experiments for which it is being intended for. The kit also have a provision where the CMOS integrated circuit (IC), which is being experimented on, would be directly connected. When the connections are completed, the power supply is then turned on. The various inputs to the CMOS integrated circuit (IC) pins could then be controlled from the input switches on the laboratory kit. Thereafter, the output of the CMOS IC could then be monitored from the indicating LED's on the laboratory kit.

So, basically, that is what the CMOS laboratory kit is all about. It is simple to use and very practical. It also goes without saying that it is a very useful laboratory equipment to both the student and lecturer. Thus, it is recommended that the department laboratory should have it.

1.2 Objectives

The primary objective of carrying out this project is to fulfill the obligatory requirement of the final year project in the award of the Bachelor's Degree in Engineering.

That been said, however, there are other reasons for carrying out the project. These other objectives are:-

1. The project, CMOS laboratory kit, is carried out to serve as an experimental kit for electrical and computer engineering students, which will enable students to carryout experiments on the investigation and demonstration of the operation of CMOS integrated circuits and logic gates.
2. The project is carried out because all the materials needed for its construction could be found locally. Thus, the price of implementation is relatively low.
3. The project is carried out in order to gain experience in the design and construction of electrical / electronics devices.
4. The project is also carried out so as to harness skills and techniques in the design and construction of electrical / electronics devices.
5. Lastly, the project is carried out so as to put into practice the theories learned over the years in the Electrical and Computer engineering programme.

1.3 Methodology

The project took a period of about three months to complete. Thus, it is only rational that it was done in a piece – meal manner i.e. step-by-step. The various steps / stages taken from inception to complete the project are:

Step 1: Firstly, the project topic was chosen after due consideration with the supervisor. The project topic was chosen on the basis of its usefulness (to the student, department, university and the world at large) and its creativity.

Step 2: Secondly, researches was taken into previous works of others in the area of study related to the project topic. These researches were done at the university library, the department (i.e Electrical and Computer Engineering) library and on the internet. The research materials were gotten from textbooks, handbooks, journals, past projects and various articles on the internet.

Step 3: Thirdly, the scope of the project was outlined after due consultation with the supervisor. This was done in order to allow for proper planning and budgeting in carrying out the project.

Step 4: Fourthly, all the materials and components needed for the project design and construction were identified and obtained.

Step 5: Fifthly, the design and construction of the project was carried out, starting from the power supply.

Step 6: Sixthly, tests and troubleshooting of the project was carried, with modifications where necessary.

Step 7: Then the experiments for which the project were meant for (set in the scope of the project) were carried out and properly documented.

Step 8: Lastly, the technical report of the project was written.

1.4 Scope of the project

Theoretically. The project has no limit to its scope except that it is meant for all CMOS integrated circuits. However, due to a number of factors which include financial factor, time factor etc., for the purpose of this project, the scope of the CMOS laboratory kit would be limited to the investigation and demonstration of the operations of the following CMOS integrated circuits and logic gates:-

i. 4011 2 – input NAND gates

ii. 40001 2 – input NOR gates

iii. 4081 2 – input AND gates

iv. 4071 2 – input OR gate

v. 4013 D – type flip flop

vi. 4518 Binary / decode counter

vii. 4070 2 – inputs Ex – OR gate

viii. 4069 Hex NOT gate

However, if different CMOS integrated circuits, other than the ones named above, are needed to be experimented on, provisions are made on the project to accommodate components that will enable the new experiments. Thus, it can be said that the scope of the project can be expanded.

1.5 Sources of Materials

The materials used for the project can be categorized into two viz; the software and the Hardware.

The software involves the research knowledge used in doing the project. These were obtained from the research materials such as textbooks, journals and articles which are available at the university and department library and on the internet.

While the hardware involves the physical materials and components used in the construction of the project. The components were obtained from electronic component shops. The other materials like the plastic, metal parts etc. were obtain from various hardware shops.

1.6 Limitations

The project being simple and very practicable to implement has little or no limitations. The only main constraint to its achievable performance is faulty / defective components.

While other limitation (which is minor and has no constraint on the achievable performance) is the lack of sophisticated fabrication technique. That is to say that with superior fabrication processes the appearance (i.e. packaging) of the project could be highly improved.

Chapter Two

Literature Review / Theoretical Background

The CMOS (digital) laboratory kit is a device which is designed mainly to investigate CMOS integrated circuits. That is to say that the CMOS laboratory kit is build on the basis of the properties and operations of CMOS integrated circuits. Therefore, the CMOS, in general, has to be understood. Thus, its literature review and theoretical background is given in the following pages.

2.1 Literature Review

The CMOS (Complementary Metal–Oxide Semiconductor) is a major class of integrated circuit. CMOS chips include microprocessor, microcontroller, static RAM, and other logic circuits [1].

The word "complementary" refer to the fact that the design uses complementary pairs of P–type and n–type MOSFET (i.e metal–oxide semiconductor field effect transistors) transistors for logic functions, only one of which is switched on at any time [2, 3].

Two important characteristics of CMOS devices are high noise immunity and low static power supply drain. Significant power is only drawn when its transistors are switching between on and off states; consequently, CMOS devices do not produce as much as heat as other forms of logic such as TTL (i.e. transistor–transistor logic) [4]. CMOS also allows a high density of logic functions on a chip [5].

The phrase "metal-oxide–semiconductor" is a reference to the nature of the fabrication process originally used to build CMOS chips. That process created field effect transistors having a metal gate electrode placed on top of an oxide insulator, which in turn

is on top of a semiconductor material. Instead of metal, today the gate electrodes are almost always made from a different material, polysilicon, but the name CMOS nevertheless continues to be used for the modern descendants of the original process [6].

2.2 Historical Background

CMOS circuits were invented in 963 by Frank Wanlass at Fairchild Semiconductor [7,8]. The first CMOS integrated circuits were made by RCA in 1968 by a group led by Albert Medwin. Originally a low power but slow alternative to TTL, CMOS found early adopters in the watch industry and in other fields where battery life was more important than speed. Some twenty–five years later, CMOS has become the predominant technology in digital integrated circuits. This is essentially because area occupation, operating speed, energy efficiency and manufacturing costs have benefited and continue to benefit from geometric downsizing that comes with every new generation of semiconductor manufacturing process. In addition, the simplicity and comparatively low power dissipation of CMOS circuits have allowed for integration densities not possible on the basis of bipolar junction transistors.

Standard discrete CMOS logic functions were originally available in the 4000 series of logic integrated circuits. Later many functions in the 7400 series began to be fabricated in CMOS, NMOS, BiCMOS or another variant [9].

Early CMOS circuits were very susceptible to damage from electrostatic discharge [ESD] [10,11]. Subsequent generations were thus equipped with sophisticated protection circuitry that helps absorb electric charges with no damage to the fragile gate oxides and PN-junctions. Still, antistatic handling precautions for semiconductor devices continue to be followed to prevent excessive energies from building up. Manufacturers recommend using antistatic precautions when adding a memory module to a computer, for instance.

On the other hand, early generations such as the 4000 series that used aluminium as a gate material were extremely tolerant of supply voltage variations and operated anywhere from 3 to 18 volts DC. For many years, CMOS logic was designed to operate from the then industry-standard of 5v imposed by TTL. By 1990, lower power dissipation was usually more important than easy interfacing to TTL, and CMOS voltage supplies began to drop along with the geometric dimensions of the transistors. Lower voltage supplies not only saved power, but allowed thinner, higher performance gate insulators to be used. Some modern CMOS circuits operate from voltage below one volt.

In the early fabrication processes, the gate electrode was made of aluminium. Later CMOS processes switched to polycrystalline silicon ("polysilicon"), which can better tolerate the high temperatures used to anneal the silicon after ion implantation. This means that the gate can be put on early in the process and then used directly as an implant mask producing a self aligned gate (gates that are not self aligned require overlap which increases device size and stray capacitance). As of 2004 there is some research into using metal gates once again, but all commonly used processes have polysilicon gates. There is also a great deal of research going on to replace the silicon dioxide gate dielectric with a high k-dielectric material to combat increasing leakage currents [12].

2.3 Theoretical Background

CMOS (Complementary metal-oxide semiconductor) refers to both a particular style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS logic on a CMOS process dissipates less energy and is more dense than other implementations of the same functionality. As this advantage has grown and become more important, CMOS processes and variants have

come to dominate, so that as of 2006 the vast majority of integrated circuit manufacturing by money volume is on CMOS processes.

2.3.1 Structure

CMOS logic uses a combination of P-type and n–type metal–oxide semiconductor field effect transistors (MOSFETS) to implement logic gates and other digital circuits found in computers, telecommunications and signal processing equipment. Although CMOS logic can be implemented with discrete devices (for instance, in an introductory circuit class), typical commercial CMOS products are integrated circuits composed of millions (or hundreds of millions) of transistors of both types on a rectangular piece of silicon of between 0.1 and 4 square centimeters. These bits of silicon are commonly called chips, although within the industry they are also referred to as die, perhaps because they are the result of dicing (i.e. cutting up) the silicon wafer which is the basic unit of semiconductor device fabrication.

In CMOS logic gates, a collection of n–type MOSFETS is arranged in a pull–down network between the output and the lower-voltage power supply rail (often named V_{ss}), while a collection of p–type MOSFETs is arranged in a pull-up network between the output and the higher-voltage rail (often named V_{dd}) [13]. The p-type transistor network is complementary to the n–type transistor network, so that the n-type is off, the p–type is on, and vice- versa.

CMOS logic dissipates power only when switching (dynamic power). P- type MOSFETs are complementary to n–type because they turn on when their gate voltage goes sufficiently below their source voltage, and because they can pull the drain all the way to V_{dd}. Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be on when the n–type MOSFET is off, and vice–

versa. The circuit diagrams of a p-type MOSFET, n-type MOSFET and CMOS are shown below.

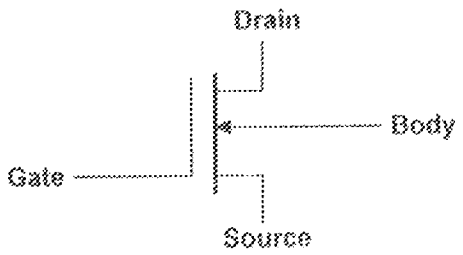

Fig. 2.2 (a) n – channel MOSFET

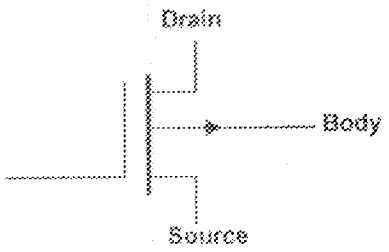

Fig. 2.2 (b) p – channel MOSFET

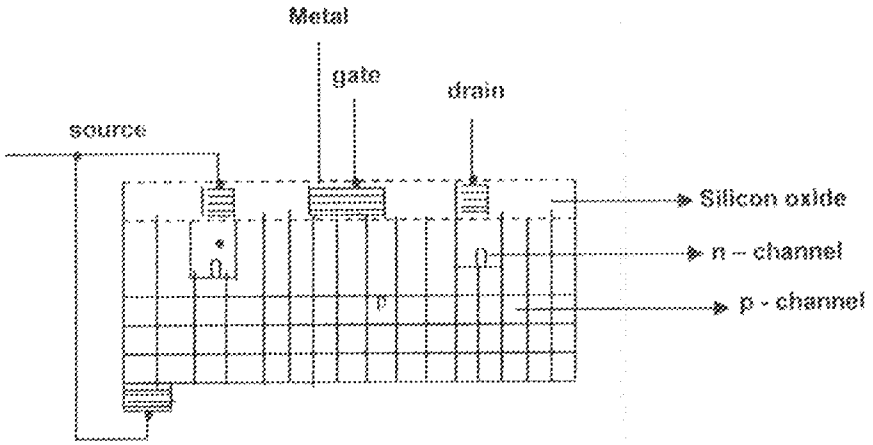

Fig. 2.2 schematic internal structure of an n – channel MOSFET

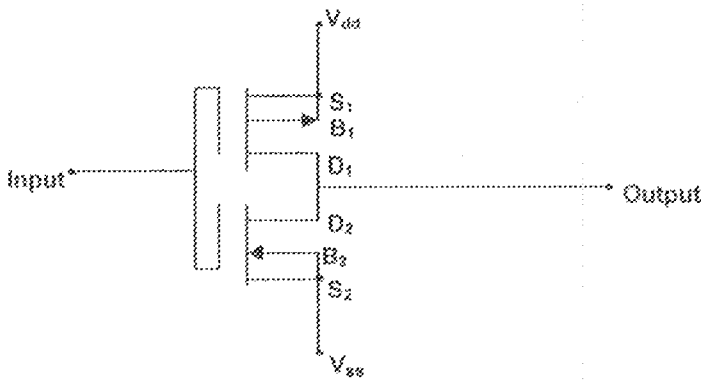

Fig. 2.3 circuit diagram of CMOS [14].

2.3.2 Power: Switching and leakage

CMOS circuits dissipate power by charging and discharging the various load capacitances (mostly gate and wire capacitance, but also drain and some source capacitance) whenever they are switched [15]. The charge moved is the capacitance multiplied by the voltage. i.e

$$Q = CV$$

Where Q is charge, C is capacitance and V is voltage change. The current used is derived by multiplying the charge with switching frequency i.e

$$I = Qf = Cvf$$

And multiplying the current used, I by voltage, v gives the characteristics switching power dissipated by a CMOS device i.e

$$p = IV = CV^2f$$

A different form of power consumption however, exists as wires on the chips become narrower and the long wires became more resistive. CMOS gates at the end of those resistive wires see slow input transition. During the middle of these transitions, both the n-type and p-type MOSFETs networks are partially conductive and current flows directly from V_{dd} to V_{ss}. The power thus used is called crowbar power [16]. Careful design which avoids weekly driven long skinny wires has ameliorated this effect, and crowbar power is nearly always substantially smaller than switching power.

Both n-type and p-type MOSFETs have a threshold gate-to-source voltage, below which the current throogh the device drops exponentially. Historically, CMOS designs operated at supply voltages much larger than their threshold voltages (V_{dd} might have been 5v and V_{th} for both n–type and p–type MOSFETs might have been 700MV). But as supply voltages have come down to conserve power the V_{dd} to V_{ss} short circuit is avoided.

However, to speed up the designs, manufacturers have switched to gate materials which lead to lower voltage thresholds and a modern n–type MOSFET with a V_{th} of 200MV has a significant sub threshold leakage current. Designs (e.g. desktop processors) which try to optimize their fabrication process for minimum power dissipation during operation have been lowering V_{th} so that leakage power begins to approximate switching power. As a result, these devices dissipate considerable power even when not switching. Leakage power reduction using new material and system design is critical to sustaining scaling of CMOS.

The industry is contemplating the introduction of high k-Dielectrics to combat the increasing gate leakage current by replacing the silicon–dioxide that are the conventional gate dielectrics with materials having a higher dielectric constant.

2.3.3 CMOS Characteristics

The CMOS logic has many nice characteristics which makes it the logic of choice and hence its dominance in the industry. These characteristics are:

i. Supply voltage

CMOS logic has a wide range of supply voltages. The HC and AC CMOS families require a supply voltage of +2 to +6 volts, whereas the 40000B and 74C CMOS families require a supply voltage of +3 to +15 volts. Yet, the HCT and ACT CMOS families, designed for compatibility with bipolar TTL, requires +5 volts.

ii. Input

CMOS logic has threshold voltage nominally at half the supply voltage (though with considerate spread, typically 1/3 to 2/3 the supply voltage). The HCT and ACT

CMOS families are designed with a low threshold similar to bipolar TTL for compatibility, since a bipolar TTL output does not swing all the way to +5 volts.

The CMOS, unlike the TTL, has no input current. CMOS inputs are susceptible to damage from static electricity during handling. Thus unused inputs should be tied high or low, as necessary. See fig. 2.4.

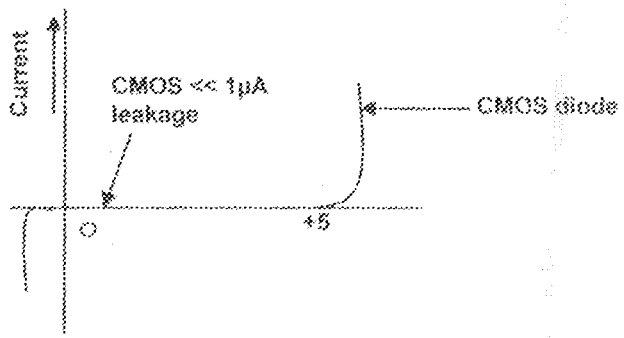

Fig. 2.4 CMOS input characteristics

iii. Output

The CMOS output stage is a turned-on MOSFET, either to ground or to V+ i.e., rail-to-rail output swings. This also applies to the HCT and ACT CMOS families which are designed for compatibility with TTL. In general, faster families (AC, ACT) have greater output drive capability than the than the slower families (4000B, 74C, HC, HCT).

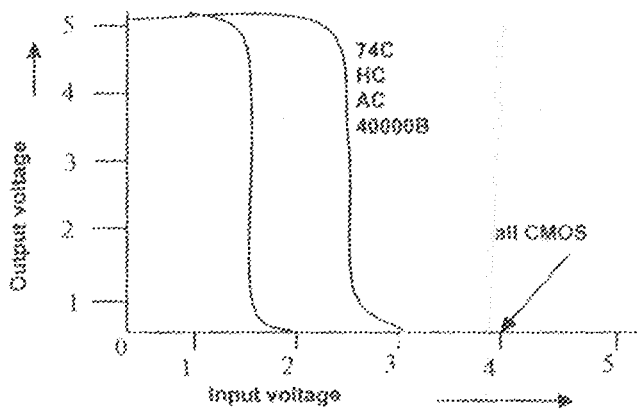

Fig. 2.5 CMOS output characteristics

iv. **Speed and Power**

The CMOS logic consumes zero quiescent current. However, their power consumption rises linearly with necessary frequency (switching capacitive loads requires current), and CMOS operated near its upper frequency limit often dissipates as much power as the equivalent bipolar TTL family. The speed range of CMOS goes from about 2MHz (for 4000B/74C at 5v) to about 100MHz (for AC/ACT). See fig. 2.6.

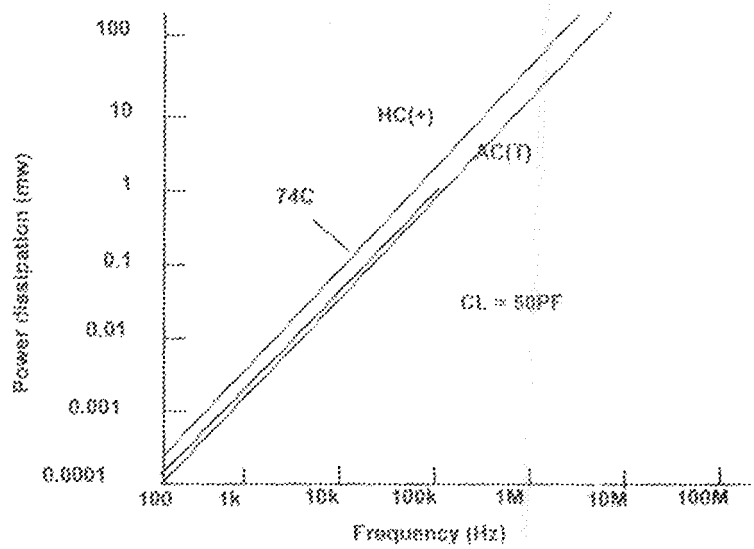

Fig. 2.6. Gate power dissipation versus frequency (speed)

2.3.4 CMOS Logic families

The CMOS logic is available in 6 popular subfamilies: 4000B, 74C, 74HC, 74HCT, 74AC, 74ACT. Thy all offer the same functions and with a pretty good degree of compatibility between them. The differences have to do with speed, power dissipation, output drive capability and logic levels. The characteristics of the various CMOS logic families are given in table 2.1 below [19].

The 4000B–series CMOS was the first CMOS logic to be developed, in 1970 [20]. This was followed by the 74C series which is essentially the same but with 74family functions and points taking advantage of the tremendous success of the 74–family bipolar

logic. During the 1980s came the remarkable development of CMOS logic with the speed and output drive of TTL: first 74HC ("High-speed CMOS") with the same speed as 74LS; then 74AC ("Advanced CMOS") with the same speed as 74F or 74 ACT. Then each of the CMOS family is offered in a variant with the lower input threshold so as to facilitate compatibility with older TTL. These variants are the 74HCT ("High-speed CMOS with TTL threshold") and the 74ACT ("Advanced CMOS with TTL threshold"). The best type for most applications is currently the 74HC-series.

Table 2.1 CMOS logic families' characteristics

Family	F max (MHz)	Pdiss @ 1 MHz (mw/gate)	IOL@ 0.5v max (MA)	IIL max (MA)	V_{in} type (v)	V supply			Date of introduction
						Min (v)	nom (v)	Max (v)	
AC	125	0.5	24	0	V+/2	2	5 or 3.3	6	1985
ACT	125	0.5	24	0	1.4	4.5	5	5.5	1985
HC	30	0.5	8	0	V+/2	2	5	6	1982
HCT	30	0.5	8	0	1.4	4.5	5	5.5	1982
4000B/74C @ 5v	2	0.3	0.5	0	V+/2	3	5-15	18	1970

Chapter Three

Design and construction

The design and construction of the CMOS laboratory kit was carried out in basically two different parts which are:

i. The power supply

ii. The CMOS laboratory kit board

The general block diagram of the CMOS laboratory kit shown below illustrates the different parts (or blocks).

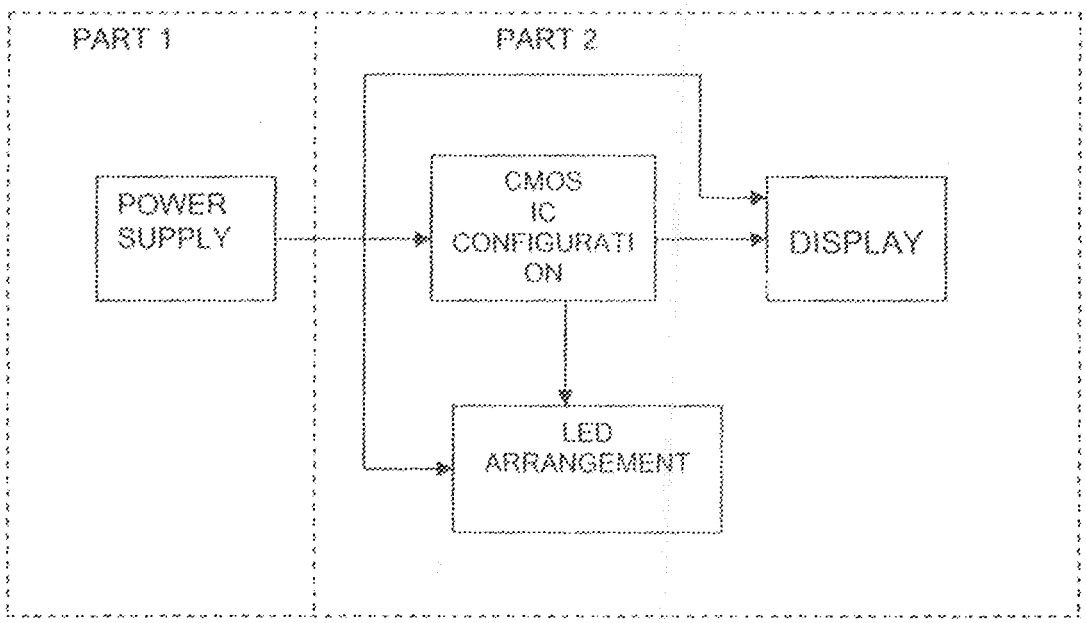

Fig. 3.1 General block diagram of the CMOS laboratory kit

3.1 The power supply

The design and the construction of the power supply to the CMOS laboratory kit were done separately. The design was first done and then it was implemented for the construction of the CMOS laboratory kit.

3.1.1 Design of the power supply

The power supply was designed specifically to facilitate use with CMOS IC's. Hence it was designed with respect to the features of CMOS IC's. CMOS IC's, as earlier said, work with a wide range of voltages ranging from 2v to 15v. Thus, the power supply was designed to produce the voltages: 3v, 5v, 9v and 12v, in DC from the 240v AC obtainable from the mains. To achieve this, a linear power supply design was used. The circuit diagram of the power supply is shown below:

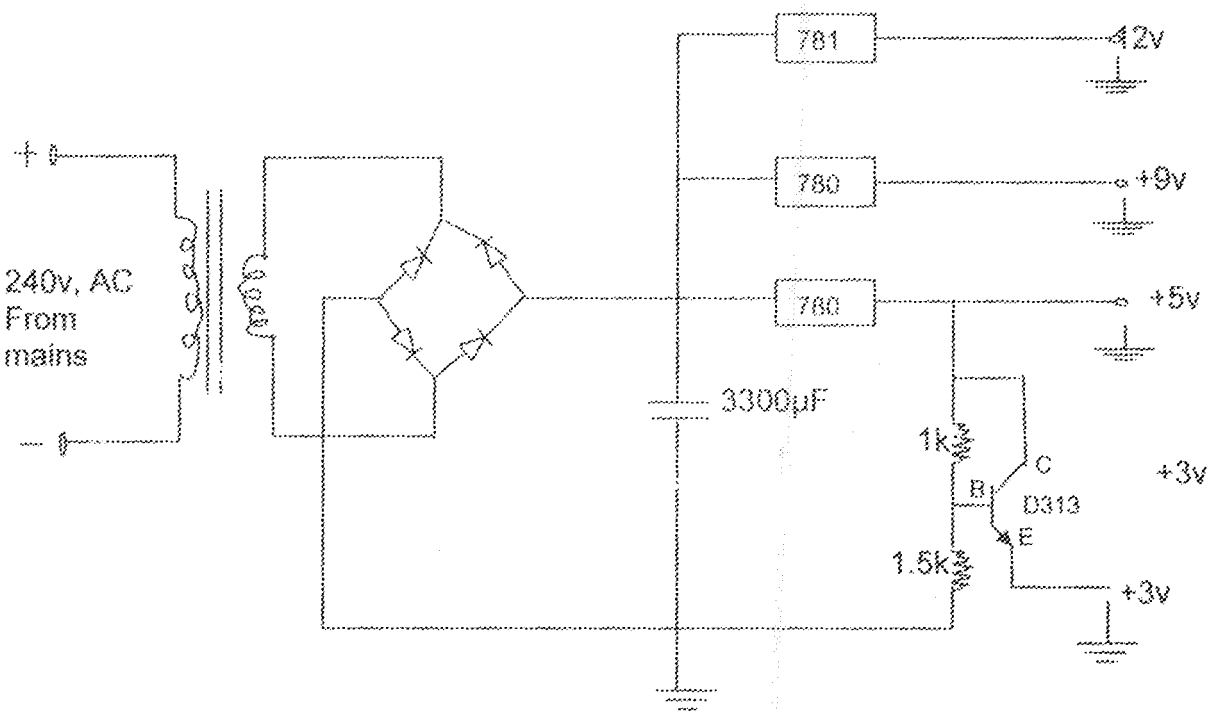

Fig. 3.2 Power supply circuit diagram

The first stage of the power supply circuit is the transformer stage. At this stage, the 240v AC from the mains is stepped down to 15v by the transformer.

The next stage is the rectification stage. At this stage the 15v from the secondary end of the transformer is rectified to a direct current voltage by the rectifier. The rectifier is a full wave bridge rectifier designed with a bridge network of four diodes. The waveform of the rectified output of the rectifier is shown below.

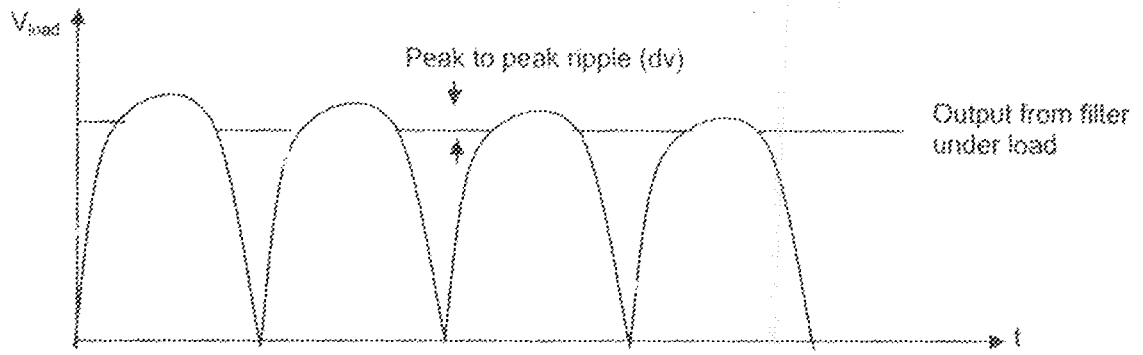

Fig. 3.3 output waveform of rectifier

The gate at zero voltage occurs because of the diodes forward voltage drop. However the rectified waveform isn't good for much as it should. It is DC only in the sense that it does not change polarity. Thus, in order to generate a genuine Dc, the ripple of the waveform has to be smoothed out. Thus is done in the next stage.

In the filtering stage, a filtering capacitor is employed to smoothing out the ripples of the waveform. The capacitance of the filtering capacitor employed is chosen to be inversely proportional to the ripple gradient of the power supply [21]. Thus, the following calculations were made to choose a suitable filtering capacitor for the power supply.

For an rms voltage of 15 volts 9from the output of transformer)

$$\text{Vpeak} = \sqrt{2}\, r.m.s = \sqrt{2}\ X\ 15$$
$$= 21.2v$$

Assuming a peak-to-peak ripple voltage of 15% the peak voltage, we have

$$dv = 15\%\ X\ 21.2 \qquad And\ ,\quad C = I\frac{dt}{dv}$$
$$= 3.18\,v$$

—> I = maximum current in circuit 1A

Dt = time between peaks of ac voltage

= ½ T (for a full-wave rectifier)

= ½ 1/f (where *f* is frequency of ac voltage i.e 50 Hz)

$$= \frac{1}{2} X \frac{1}{50} = 0.01s$$

$$\therefore C = I \frac{dt}{dv} = \frac{1 \times 0.01}{3.18} = 3225.8\mu f.$$

So, a 330μf capacitor which is the closest to 3225.8μf available) was employed as he filtering capacitor.

Lastly, the final stage of the power consists of the voltage regulators. The need for voltage regulators arises from the fact that there is still some remaining ripple in the output from the filter. The voltage regulators hold the outputs at the required values regardless of the input voltage variations. Hence, 7805, 7809 and 7812 voltage regulator IC's were used to provide +5v dc, +9vdc and +12vdc voltage outputs respectively. However, a voltage regulator IC for 3v dc was unavailable, hence and alternative method was used.

The 3v dc output was achieved by using a transistor configuration whereby the emitter of the transistor was biased approximately to produce a 3v supply. The power transistor used is D313 npn transistor. The transistor configuration is shown below.

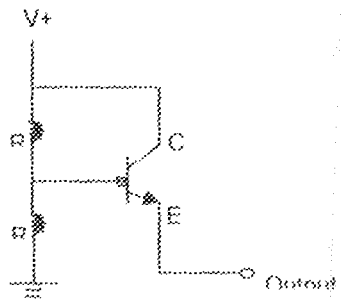

Fig. 3.4 Transistor configuration to obtain 3v

The value of the resistors R_1 and R_2 used were determined from the following calculations.

The resistor $R_1$and R_2 from a potential divider network, hence:

$$V_{out} = \frac{R_2 V_+}{R_1 + R_2}$$

The transistor configuration connected to 5v dc, hence v+ is 5v. The output desired is 3v and R_1 is assumed to be 1kΩ. Therefore

$$3v = \frac{R_2 X 5}{1k_1 + R_2}$$
$$\Rightarrow 3k + 3R_2 = 5R_2$$
$$2R_2 = 3k$$
$$R_2 = 1.5k\Omega$$

Therefore, 1Ω and 1.5kΩ resistors were used in the transistor configuration to provide the 3vdc output.

3.1.2 Construction of the Power supply

The power supply was constructed after its design was completed. It was constructed in the stages according to how it was designed. The components used for the construction are:

i. 15v step – down transformer

ii. Full – wave bridge rectifier (4 diodes)

iii. 3300μF capacitor

iv. Lm 7805 voltage regulator IC

v. LM 7809 voltage regulator IC

vi. LM 7812 voltage regulator IC

vii. D313 npn transistor

viii. 1kΩ, 1.5kΩ resistors

The construction procedure steps taken are as follows:

- The transformer leads were soldered to a vero board.

- A bridge network of four diodes was connected to form the full-wave bridge rectifier. Then the full-wave bridge rectifier was connected (by soldering) to the leads of the transformer, appropriately. Furthermore, one terminal of the full-wave bridge rectifier was grounded.
- The 3300μF filtering capacitor was then connected to the output of the full-wave bridge rectifier by the positive terminal whereby the negative terminal was grounded.
- Therefore, the 7812, 7809 and 7805 voltage regulator IC's were connected. Their respective input terminals were connected to the output of the filtering capacitor and the ground ends were grounded. Their output gives the required 12v, 9v and 5v dc supply.
- The D313 npn transistor was connected to the 5v supply with the collector terminal. Then the 1kΩ and 1.5kΩ were connected to the collector-base and base-emitter circuits respectively. The transistor was grounded by the base terminal while the emitter terminal gives the 3v dc supply required.
- Plugs were connected to the voltage regulator IC's so that any required voltage supply needed can be readily plugged into a socket provided from which power is drawn to the CMOS IC's.
- Lastly, a switch and an indicator LED were connected. The switch's purpose is to control the supply of power while the LED indicates if the power is supplied or not.

3.2 The laboratory kit board

The laboratory kit board is the main body of the CMOS laboratory kit. In fact, it is the essence of the project. It is on the laboratory kit board that the experiments would be performed on. Therefore the design and subsequently the construction of the laboratory kit board was undertaken diligently.

3.2.1 Design of the laboratory kit board

The design of the laboratory kit board was an expansive. This is due to the fact that the CMOS laboratory kit was intended for various experiments to investigate and demonstrate the operation of a number of different CMOS IC's. The CMOS IC's to be experimented on are:

i. 4001 2-input NOR gates

ii. 4011 2-input NAND gates

iii. 4081 2-input AND gates

iv. 4071 2-input OR gates

v. 4013 D type flip-flop

vi. 4069 hex NOT gates

vii. 4070 2 input Ex – OR gates

viii. 4518 Dual decade (0-9) counter

Therefore the design of the laboratory kit board has to reflect the individual operations of the CMOS IC's mentioned above. These operations of the CMOS IC's are now outlined below:

i. 4001 2-input NOR gates [22]

The 4001 has four separate 2-input NOR gates which can be used independently. The pin connection of the 4001 is shown below:

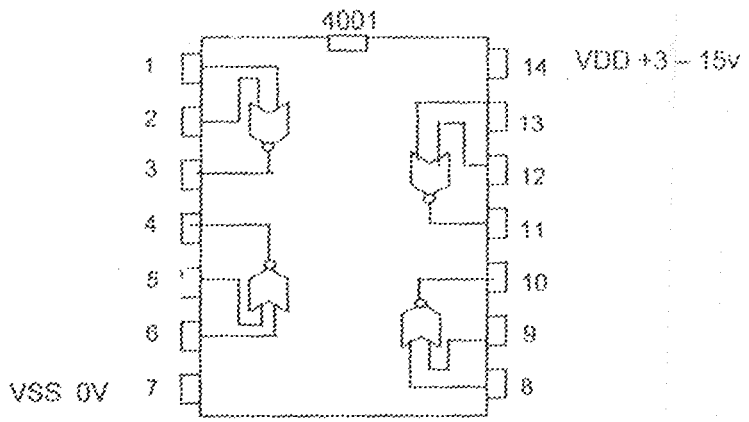

Fig. 3.4 4001 pin connections

The truth table of each individual gate is:

Table 3.1. Truth-table of a NOR gate.

Input B	Input A	Output
0	0	1
0	1	0
1	0	0
1	1	0

Where 'O' represents a low voltage and '1' represents a high voltage. The behavior of a single NOR gate can be investigated using this circuit shown below.

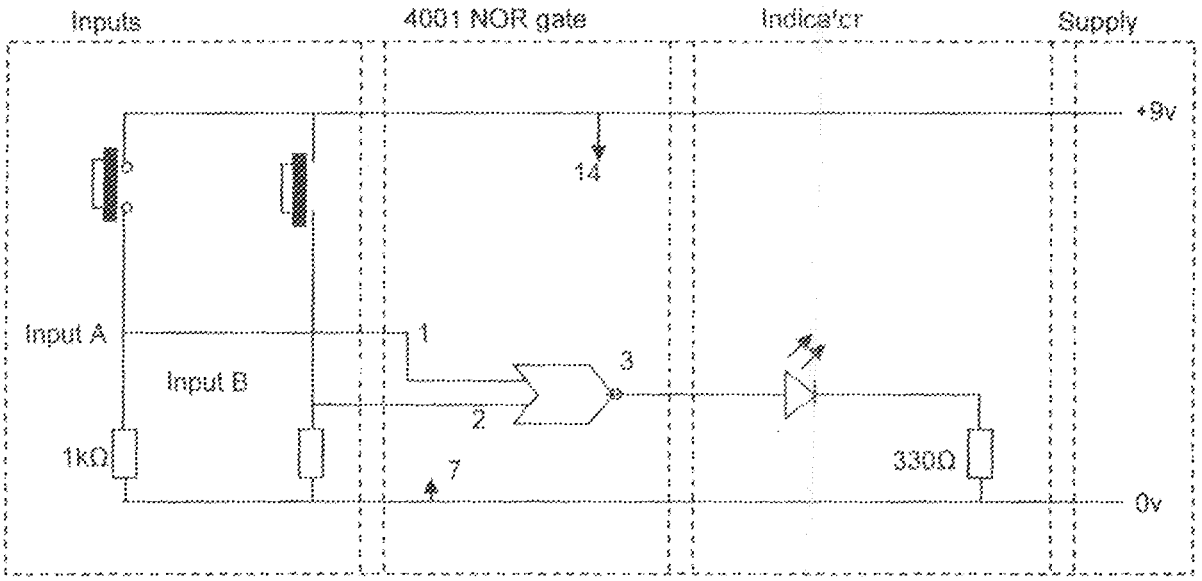

Fig. 3.5 Circuit diagram for investigation of NOR gate behaviour

The inputs of the gate must be connected either to low or to high, and must not be left open circuit. This is the function of the input switches with their pull down resistors. The output of the gate is connected to an indicator LED which goes on or off depending on the combination of the inputs.

Note that pin 14 of the 4001 is connected to +9v and pin 7 to 0v.

ii. 4011 2-input NAND gates [23].

The 4011 has four separate 2-input NAND gates which can be used independently. The pin connection of the 4011 is shown below.

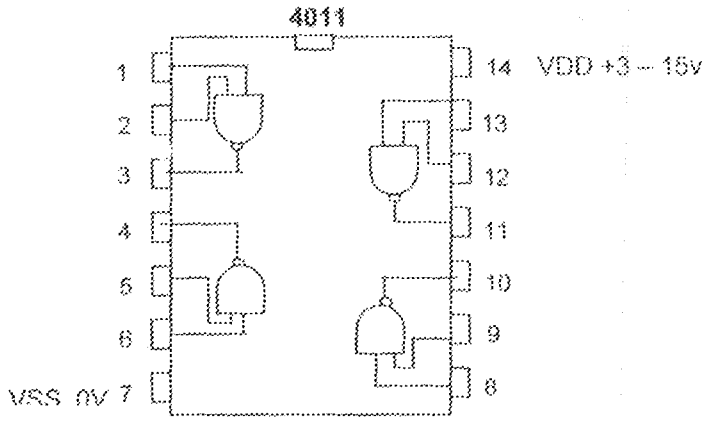

Fig. 3.6 4011 pin connections

The truth-table of each individual gate is:

Table 3.2 Truth table of a NAND gate

Input B	Input A	Output
0	0	1
0	1	1
1	0	1
1	1	0

The behaviour of a single NAND gate can be investigated using this circuit shown below:

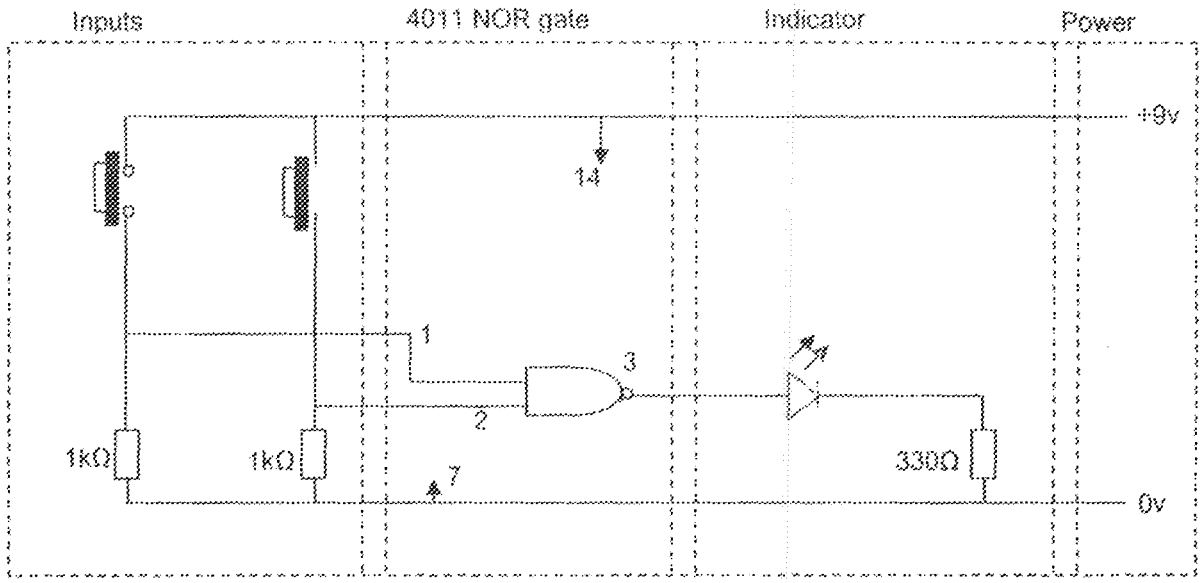

Fig. 3.7 Circuit diagram for demonstration of NAND gate operation

The inputs of the gate must be connected, either to low or to high, and must not be left open circuit. This is the function of the input switches with their pull-down resistors. The output of the gate is connected to an indicator LED which goes on or off depending on the combination of the inputs.

Pin 14 of the 4011 is connected to +9v and pin 7 to 0v.

iii. 4081 2-input AND gates [24]

The 4081 has four separate 2-input AND gates which you can use independently. The pin connection of the 4081 is shown below.

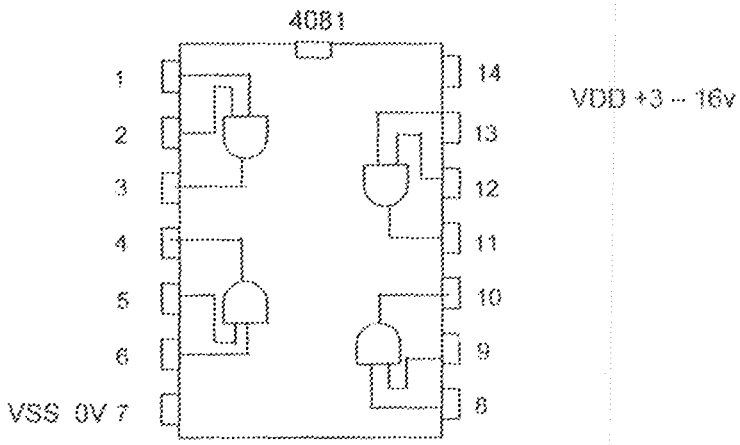

Fig. 3.8 4081 pin connections

The truth table of each individual gate is

Table 3.3 Truth table of an AND gate

Input B	Input A	Output
0	0	0
0	1	0
1	0	0
1	1	1

The behaviour of a single AND gate can be investigated using the circuit shown in fig. 3.9 below. The inputs of the gate must be connected, either to low or to high, and must not be left open circuit. This is the function of the input switches with their pull-down resistors. The output of the gate is connected to an indicator LED which goes ON or OFF depending on the combination of the inputs. Pin 14 of the 4081 is connected to +9v and pin 7 to ov

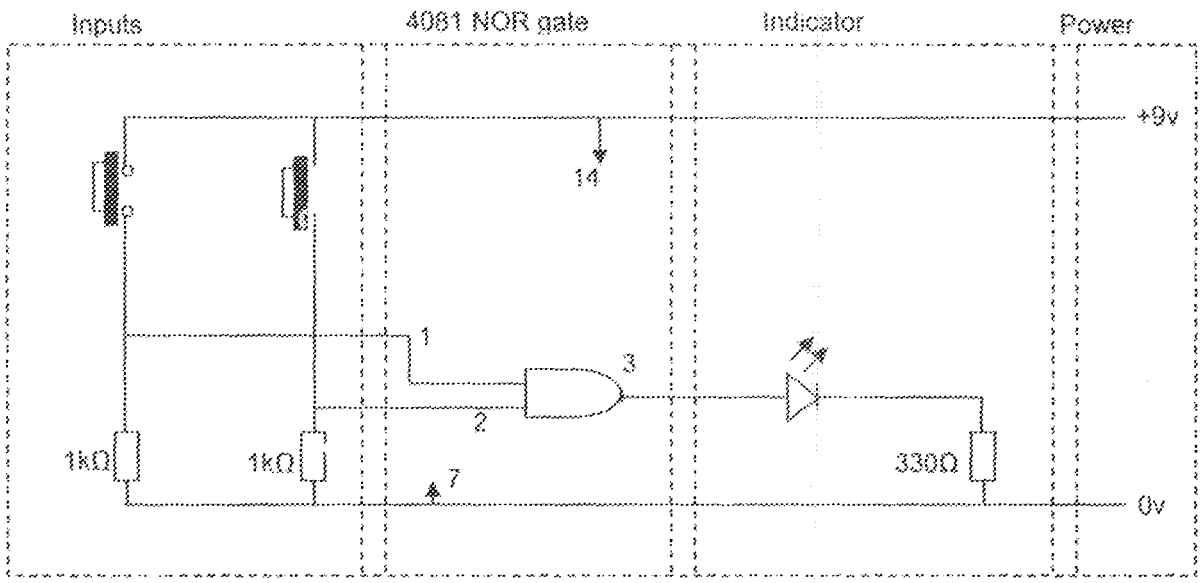

Fig. 3.9 Circuit diagram for demonstration of AND gate operation

iv. 4017 2-input OR gates [25]

The 4071 has four separate 2-input OR gates which can be used separately. The pin connection of the 4071 is shown below.

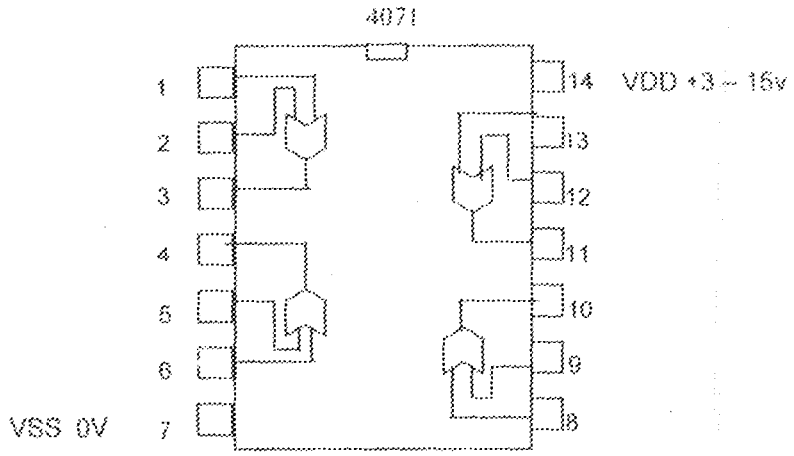

Fig. 3.4 4071 pin connections

The truth table of each individual gate is:

Table 3.4 truth table of an OR gate

Input B	Input A	Output
0	0	0
0	1	1
1	0	1
1	1	1

The behaviour of a single OR gate can be investigated using the circuit shown below. The inputs of the gate must be connected either to LOW or to HIGH, and must not be open circuit. This is the function of the input switches with their pull-down resistors. The output of the gate is connected to an indicator LED which goes ON or OFF depending on the combination of the inputs. Pin 14 of the 4071 is connected to +9v and pin 7 to 0v.

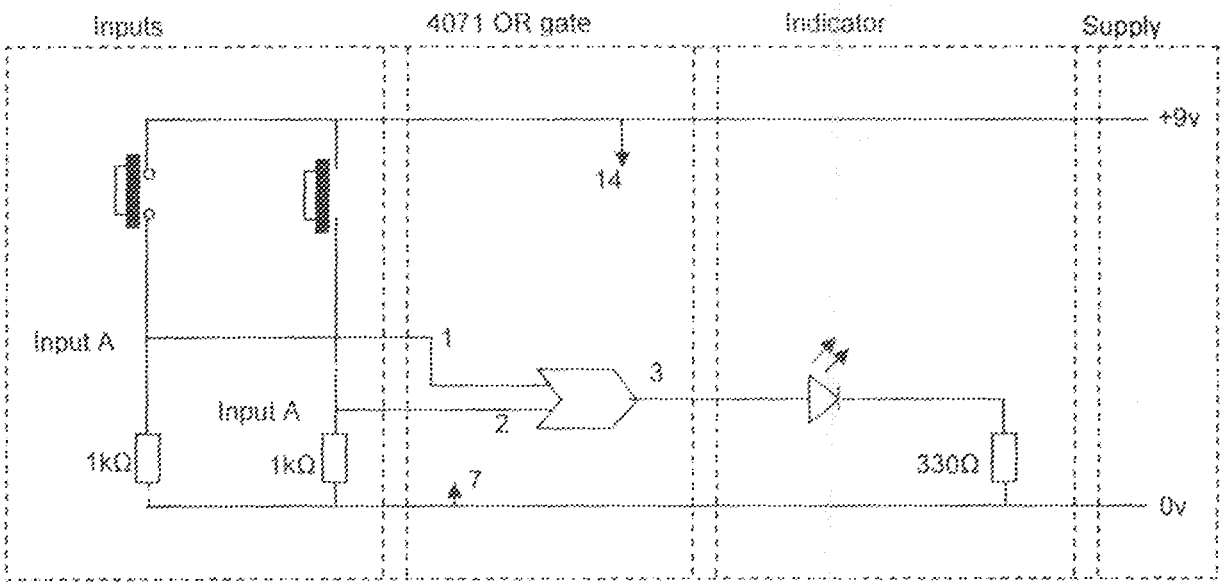

Fig. 3.11 Circuit diagram for demonstration of OR gate operation

v. 4013 D-type flip-flops [26]

The 4013 has two D-type flip-flop which can be used independently. The pin connection of the 4013 is shown in fig. 3.12 (a) below. A D-type flip-flop, also called 'D-type bistable', is a subsystem with two stable states. Using appropriate input signals, you can trigger the flip-flop from one state to another. Fig 3.12(b) shows the input and output connections of a single D-type bistable.

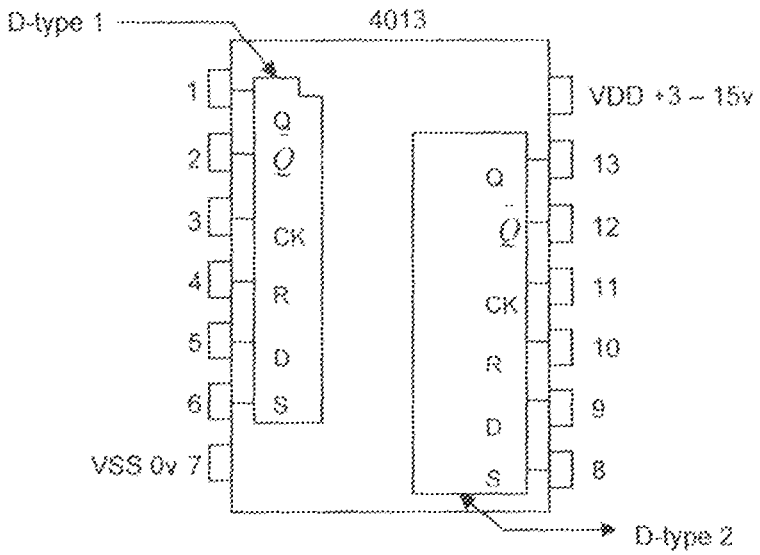

Fig. 12(a) 4013 pin connections

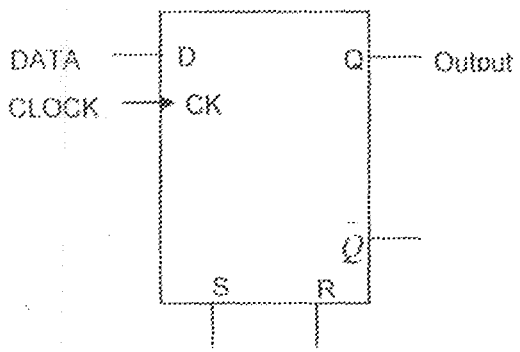

Fig. 3.12(b0 Input and output connections of a single D-type flip-flop.

The truth table of each D-type flip-flop is:

Table 3.5 truth table of a D-type flip-flop

CL+	D	R	S	Q	$\bar{Q}$
√	0	0	0	0	1
√	1	0	0	1	0
¬	X	0	0	Q	$\bar{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

No change

+ = level change

X = don't care case

Q and $\bar{Q}$ are the outputs of the bistable. The logic states of the outputs are always opposite. The bistable is SET when Q = 1 and $\bar{Q}$=0, and RESET when Q = 0 and $\bar{Q}$ = 1. The D-type has four inputs. These are:

- DATA input: This is connected either to a LOW voltage, logic 0, or to a high voltage, 1.

- CLOCK input: The triangle, → ck, next to the clock input shows that it is 'edge-triggered', that is, it responds to sudden changes in voltage, but not to slow changes or steady logic levels. The clock input of the 4013 D-type bistable is 'rising edge triggered', meaning that it responds only to a sudden change from low or high. Usually, the clock input is connected to a subsystem which delivers pulses. To test the 4013, an astable is required.

- SET input: The SET input is normally held low. When it is pulsed HIGH, the outputs of the bistable are forced immediately to the SET state, Q=1, $\bar{Q}$ = 0.

- RESET input: The RESET input is normally held LOW. When it is pulsed HIGH, the outputs of the bistable are forced immediately to the RESET state, Q=0, $\bar{Q}$ = 0.

When the D-type bistable does can be investigated by building a circuit in which the $\bar{Q}$ output is connected back to the D-input. This arrangement is called a 'toggle flip-flop', or 'toggle bistable'. The diagram below shows the circuit.

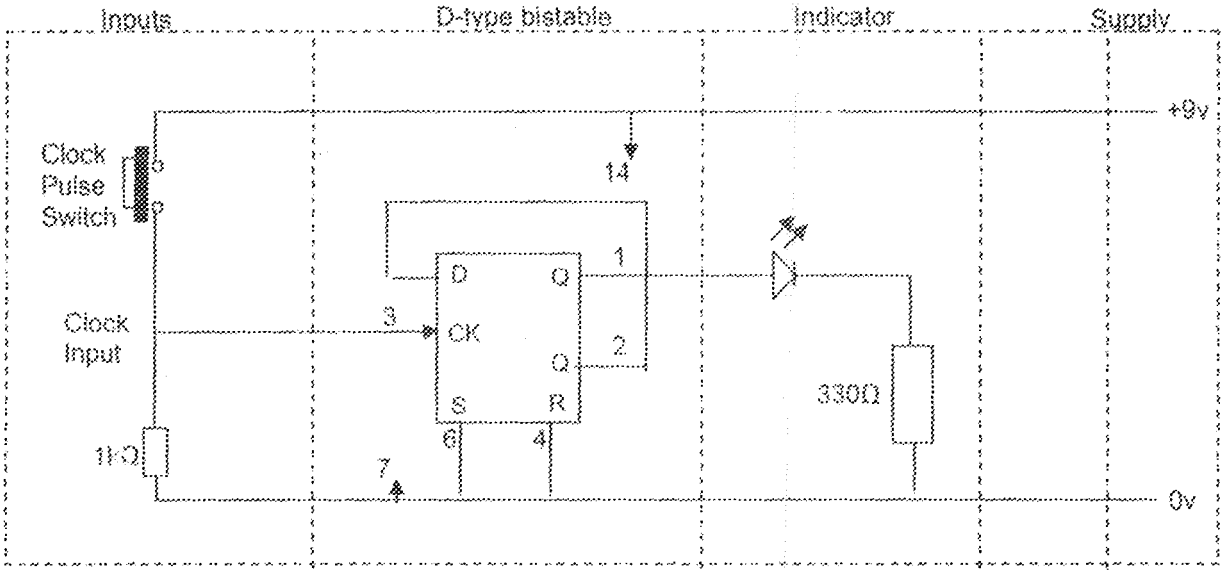

Fig. 3.13 Circuit diagram for demonstration of D-type flip-flop operation

The inputs of the D-type must be connected, either to low or high, and most not be left open circuit. This includes the SET and RESET inputs which are connected to 0v. The output of the D-type, i.e. Q is connected to an indicator LED.

vi. 4070 2-input EX OR gates [27]

The 4070 has four separate 2-input Ex-OR gates which can be used independently. The pin connections of the 4070 is shown below

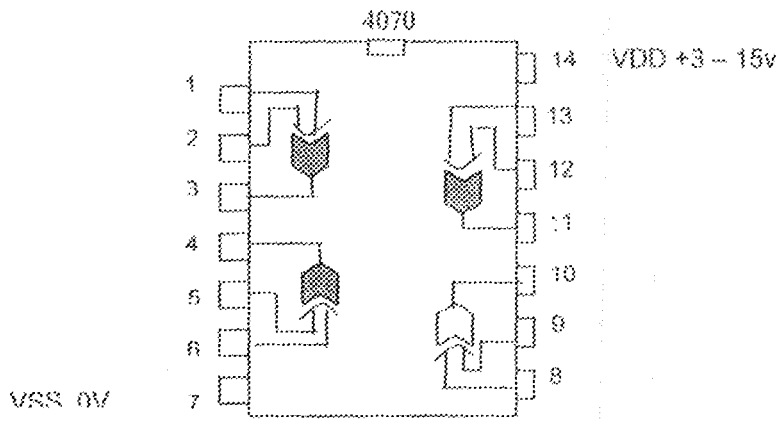

Fig. 3.14 4070 pin connections

The truth table of each individual gate is:

Table 3.6 Truth table of an Ex- OR gate

Input B	Input A	Output
0	0	0
0	1	1
1	0	1
1	1	0

The behaviour of a single Ex-OR gate can be investigated using this circuit shown below.

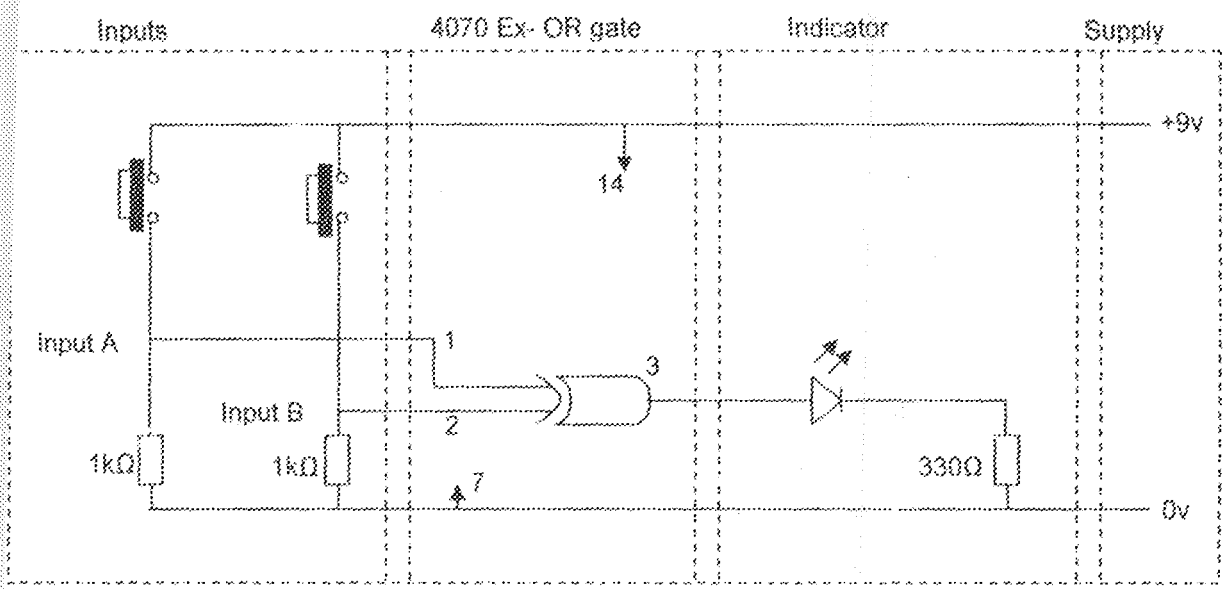

Fig. 3.15 Circuit diagram for demonstration of Ex-OR gate operation

The inputs of the gate must be connected either to low or to high, and must not be left open circuit. This is the function of the switches with their pull-down resistors. The output of the gate is connected to an indicator LED which goes on or off depending on the combination of the input.

vii. 4069 hex NOT gates [28]

The 4069 has six separate NOT gate which can be used independently. The pin connection of the 4069 is shown below.

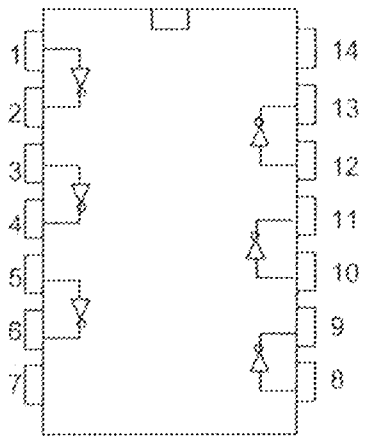

Fig. 3.16 4069 pin connections

The truth table of each individual gate is:

Table 3.7 Truth table of a NOT gate

Input B	Output
0	1
1	0

The behaviour of a single NOT gate can be investigated using the circuit shown below. The input of the gate is connected either to low or high. This is the function of the switches with their pull-down resistors. The output is connected to an indicator LED which goes on or off depending on the input.

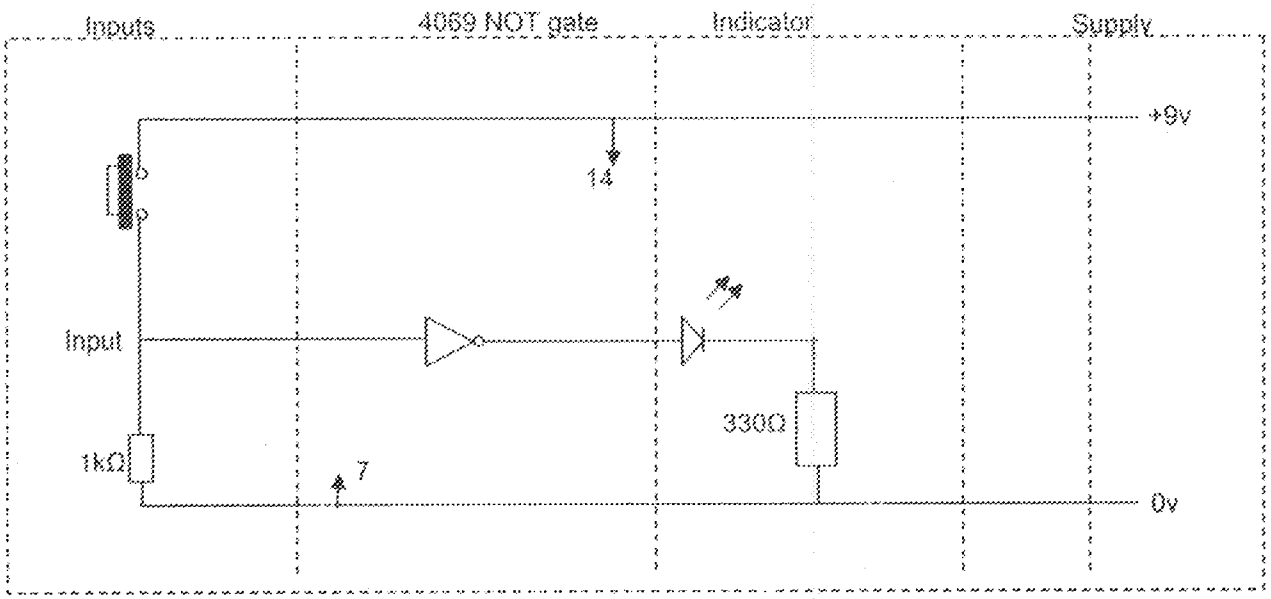

Fig. 3.17 Circuit diagram for demonstration of NOT gate operation

viii. 4518 dual decade (0-9) counter [29]

The 4518 contains two separate synchronous counters, one on each side of the chip. The pin connection of the 4518 is shown below.

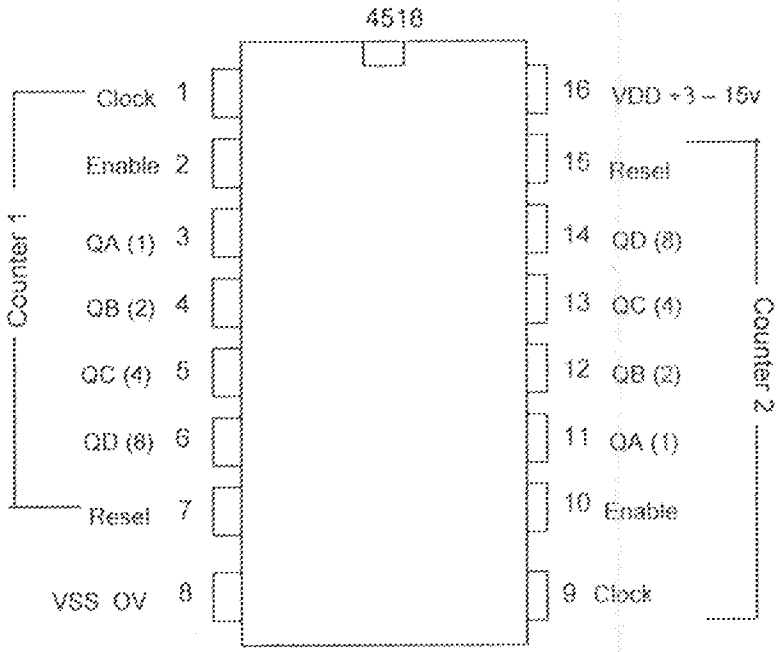

Fig. 3.18 4069 pin connections

Normally a clock signal is connected to the clock input, with the enable input held high. Counting advances as the clock signal becomes high (on the rising edge). For normal operation the reset input should be low, making it high resets the counter to zero (i.e 0000, QA-QD low).

The truth table of each counter is

Table 3.8 Truth table of a decade counter

Clock	Enable	Reset	Action
√	1	0	Increment counter
O	√	0	Increment counter
√	X	0	No change
x	√	1	Mo change
√	O	0	No change
1	√	0	No change
X	X	1	Q_1 through Q_4= O

The behaviour of a single decade counter can be investigated by the circuit shown below. A 7-segment decoder driver and display is connected to the decade counter to show the counting sequence visibly.

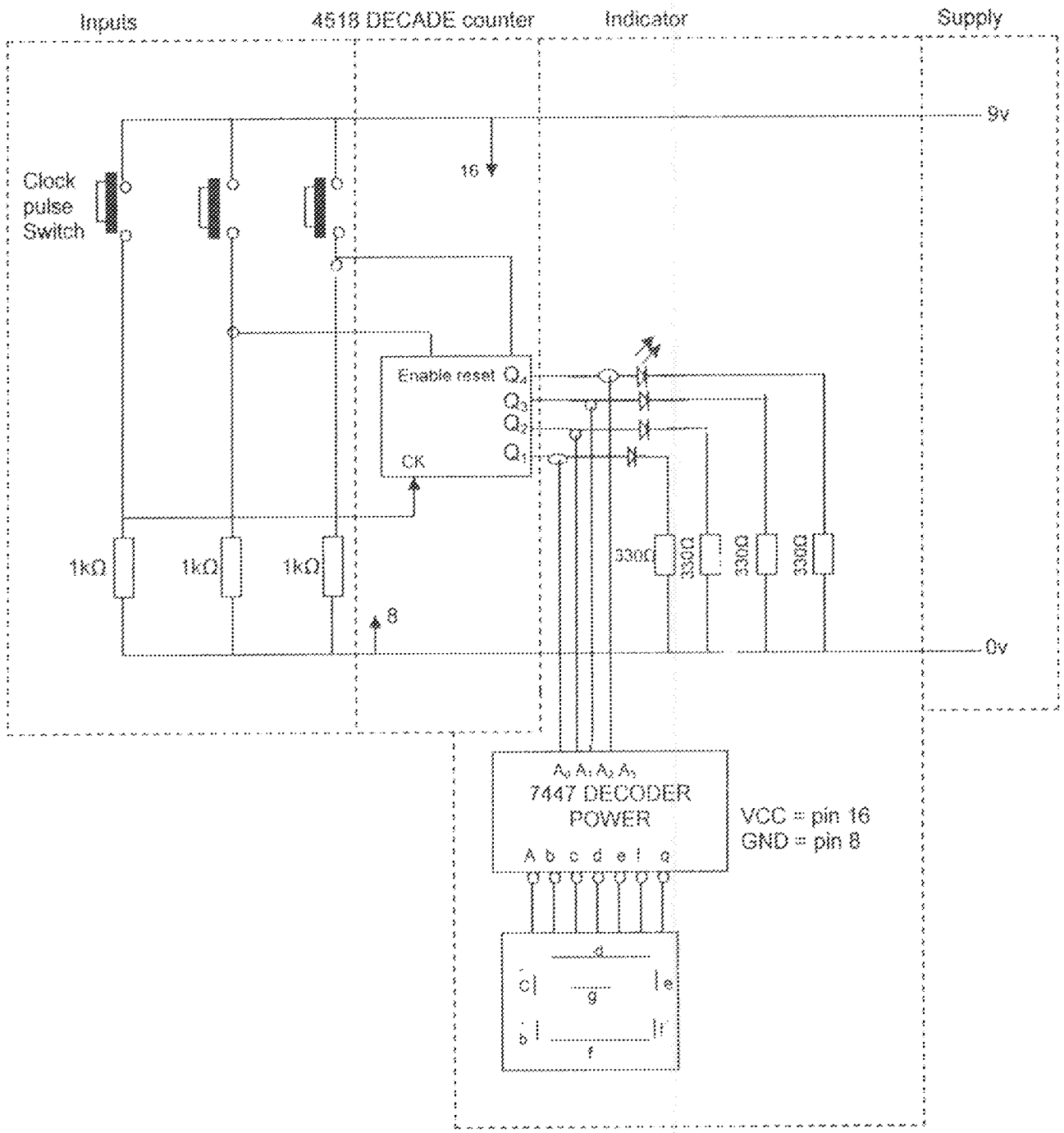

Fig. 3.19 Circuit diagram for demonstration of decade counter

3.2.2 Construction of the laboratory kit board

Te laboratory kit board was constructed in such a way that it will be possible to build the circuits for the investigation of the behaviour of the CMOS IC's. The components used for the construction of the laboratory kit board are:

i. Vero boards

ii. 14 pin IC connectors

iii. 16 pin IC connectors

iv. Push to make switches

v. Indicator LED's

vi. 1kΩ resistors

vii. 330Ω resistors

viii. Connecting wires

ix. Connecting pins (props)

x. CMOS IC's

xi. 7 segments display and decoder driver (7447)

xii. Pulse generating switches

The constructions was carried out in the following steps

- The 14 pin and 16 pin IC connectors were attached to a vero board by soldering. Pins 7 of all the 14 pin IC connectors were connected to ground while for the 16 pin IC connectors, pins 8 were connected to the ground (i.e. VSS ov). Also, pins 14 and pins 16 of the 14 pins and 16 pins IC connectors respectively were connected to the supply from the power supply unit (i.e for VDD + 3v to 15v). The supply was connected via push-to make switches so that the supply of power to the connectors can be controlled.
- A band of switches were then attached to the vero band. These switches are for the control of the input signals to the input pins of the CMOS IC's. One terminal of all the

switches were connected to the power supply while the other ends were all grounded through a 1kΩ resistor (i.e. pull-down resistor). The function of the resistor is to prevent the direct connection of the power supply with the ground by creating a voltage divider network. Then pins were connected to this terminal. These pins are the means of supplying the input signals to the input pins of the CMOS IC's.

- A couple of pulse generating switches was also attached to the board. These switches are meant for the clock inputs of the 4013 D-type flip-flop and the 4518 dual decade counter. The switches were configured in the same way as the input switches.
- Then, a baad of indicator LED's were provided by connecting the cathode terminals to connectors which were grounded through 1kΩ resistors and pins were connected to the anode terminals. The function of the LED's is to indicate the state of the output (either ON or OFF) of the CMOS IC when the pins connected to the anode of the LED's are being connected to the output pins of the IC's.
- A 7 segment display and decoder drivers were also attached to the vero board by IC connectors. These are added so as to show the output of the 4518 counter in decimal which is more easily understood. The decoder driver was connected to the 16 pin IC connector for the 4518 dual decoder (0-9) counter. Two types of decoder drivers were employed viz: a 7447 TTL decoder driver and a 74LS decoder driver. This was done to demonstrate the difference between TTL and CMOS logics i.e. CMOS logic operates over a wider range of voltage than TTL logic.

3.3 Casing

The casing is also an integral part of the project. The casing is made up of transparent plastic and consists of two levels. The lower consist of the power supply unit and the internal connections of the laboratory kit board. The upper level is the laboratory

kit board on which experiments would be carried out. It consists of the CMOS IC's and connectors, switches, indicator LED's and input pins. Then a cover is made upon the upper level so that the kit can be opened and closed. Furthermore, compartments are made were IC's and components would be stored.

Chapter Four

Tests, Results and Discussion

Each unit of the CMOS laboratory kit was tested as outlined below.

4.1 Power supply

The power supply was first tested to ensure that the required voltage supplies to power the CMOS IC's were provided.

Procedure: The test was done with a digital multimeter which was set appropriately to DC. The negative terminal and positive terminal of the power supply plugs (connected to the voltage regulator IC's) respectively. Input power from the mains to the power supply unit was switched on. The readings of the digital multimeter were recorded accordingly. The procedure was done for all the voltage regulators.

Result: The result obtained for the tests are tabulated below:

Table 4.1 Power supply test results

S/No	Voltage regulator	Recorded voltage (v)	Required voltage (v)
1	LM 7812	11.80-12.02	12v
2	Lm 7809	8.90-9.03	9
3	LM 7805	4.95-5.05	5
4	D313	2.95-3.05	3

Discussion: The recorded values from the test are not exactly as the required voltages. However they fall in the acceptable range. The discrepancies are caused by fluctuations in power supply from PHCN among other reasons.

4.2 Laboratory kit board

The laboratory kit board was tested by carrying out experiments for each of the CMOS IC's to investigate their behaviours. The testes and results obtained are as follows.

4.2.1 4001 2-input NOR gates.

Procedure: It is required to build the circuit to investigate the behaviour of a single 4001 NOR gate as shown in fig. 3.5. The steps taken are:

* The 4001 CMOS IC was inserted into a 14 pin IC connector on the board.
* The input pin props of the board were connected to the input pins of the first NOR does gate of the 4001 IC (i.e. pin 1 and 2).
* The output pin of the NOR gate of the 4001 IC was connected to an indicator Led with the aid of the pin prop connected to the anode LED.
* One of the voltage supply plug (3v) was plugged into the voltage supply socket on the board.
* The power supply unit was connected to the mains and the switch on the laboratory kit was switched ON.
* The push-to-make switch of the IC connector was pushed down (i.e. switched on).
* Then the state of the two input switches were varied between ON and OFF positions and the state of the indicator LED was recorded.
* The procedure was repeated with supply voltage of 5v, 9v and 12v.

Result: the result obtained (with all of the supply voltages) is recorded on the table below.

Table 4.2 4001 2-input NOR gate test results

Input switch	Input switch A	Indicator LED
OFF	OFF	ON
OFF	ON	OFF
ON	OFF	OFF
ON	ON	OFF

Discussion: The results obtained, shown above, satisfies the truth-table of the NOR gate in table 3.1. Thus, the project is justified.

4.2.2 4011 2-input NAND gates

Procedure: It is required to build the circuit to investigate the behaviour of a single 4011 NAND gate as shown in fig. 3.7. The same procedure as for the 4001 CMOS IC was taken with the 4011 CMOS IC.

Result: The result obtained (with all of the supply voltage) is recoded on the table below.

Table 4.3 4011 2-input NAND gate test results

Input switch B	Input switch A	Indicator LED
OFF	OFF	ON
OFF	ON	ON
ON	OFF	ON
ON	ON	OFF

Discussion: The result obtained, shown above, satisfies the truth-table of the NAND gate in table 3.2. The experiment shows the behaviour of the 4011 CMOS IC. The project is justified.

4.2.3 4081 2-input AND gates

Procedure: It is required to build the circuit to investigate the behaviour of a single 4081 AND gate as shown in fig. 3.9. The same procedure as for the 4001 CMOS IC was taken with the 4081 CMOS IC.

Result: The result of the experiment obtained is recorded on the table below.

Table 4.4 4081 2-input AND gate text results

Input switch B	Input switch A	Indicator LED
OFF	OFF	OFF
OFF	ON	OFF
ON	OFF	OFF
ON	ON	ON

Discussion: The result obtained, shown above, satisfies the truth-table of the AND gate in table 3.3. The experiment shows the behaviour of the 4081 CMOS IC

4.2.4 4071 2-input OR gates

Procedure: It is required to build the circuit to investigate the behaviour of a single 4071 OR gate as shown in fig. 3.11. The same procedure as for the 4001 CMOS IC was taken with the 4071 CMOS IC.

Result: The result of the experiment obtained is recorded on the table below.

Table 4.5 4071 2-input OR gate test results

Input switch B	Input switch A	Indicator LED
OFF	OFF	OFF
OFF	ON	ON
ON	OFF	ON
ON	ON	ON

Discussion: The result obtained for the experiment on the 4071 satisfies the truth-table of the OR gate in table 3.4. The experiment shows the behaviour of the 4071 CMOS IC.

4.2.5 4070 2-input Ex – OR gates

Procedure: It is required to build the circuit to investigate the behaviour of a single 4070 Ex – OR gate as shown in fig. 3.15. The same procedure as for the 4001 CMOS IC was taken with the 4070 CMOS IC.

Result: The result of the experiment obtained is recorded on the table below.

Table 4.6 4070 2-input Ex- OR gate test results

Input switch B	Input switch A	Indicator LED
OFF	OFF	OFF
OFF	ON	ON
ON	OFF	ON
ON	ON	OFF

Discussion: The result obtained, shown above, satisfies the truth-table of the Ex - OR gate in table 3.6. The experiment shows the behaviour of the 4070 CMOS IC and the result justifies the project.

4.2.6 4069 hex NOT gate

Procedure: It is required to build the circuit to investigate the behaviour of a single 4069 NOT gate as shown in fig. 3.17. The same procedure as for the 4001 CMOS IC was taken with the 4069 CMOS IC, but in this case with only one input switch connected to the one input of the NOT gate.

Result: The result of the experiment obtained is recorded on the table below.

Table 4.7 4069 hex NOT gate test results

Input switch	Indicator LED
OFF	ON
ON	OFF

Discussion: The result of the experiment on the 4069 obtained satisfies the truth-table of the NOT gate in table 3.7. The experiment shows the behaviour of the 4069 CMOS IC and the result justifies the project.

4.2.6 4013 D-type flip flop

Procedure: It is required to build to build the circuit to investigate the behaviour of a single D-type flip-flop as shown in fig. 3.13. The steps taken were:

- The 4013 D-type flip-flop was inserted into a 14 pin IC connector on the board
- The reset and set pins (i.e. pins 4 and 6 respectively) of the D-type flip-flop were grounded by connecting them to pin 7 of the connector.
- The $\bar{Q}$ output pin was connected back to the data input pin of the D-type flip-flop to form a 'toggle bistable'.
- The pin prop of a pulse generator switch was connected to the clock input of the D-type flip-flop 9i.e pin 3)
- An indicator LED was connected to the Q output (pin 1) of the D-type. State of the indicator LED was recorded for each pulse. This was repeated 3 times.

Result: The result of the experiment is recorded as shown in the table below.

Table 4.8 4013 D-type flip-flop test result

Clock input switch state	Indicator LED state
First push	0
Second push	1
Third push	0
Fourth push	1

Discussion: The result obtained as shown above, for the experiment satisfies the truth-table of the D-type flip- flop in table 3.5. The experiment demonstrates the operation of the D-type flip-flop.

4.2.8 4518 dual decade counter

Procedure: It is requirol to build the circuit to investigate the behaviour of the decade counter as shown in fig. 3.19. The following steps were taken.

- The 4518 IC was inserted into a 16 pin IC connector on the board
- Two input pin props were connected to the reset and enable pins (pins 7 and 2 respectively) of the first decade counter of the 4518 IC
- A pulse generator switch was connected to the clock input pin (pin 1) of the decade counter via an input pin prop.
- Four indicator LED's were connected separately to the four decade counter pins Q_A, Q_B, Q_C, Q_D (pins 3, 4, 5, 6).
- The enable input switch was switched on and the reset input switch was also switch on and then switched off. The indicator LED states were recorded along with the state of the 7 segment display (not that the 7 segment display was already connected to the 4518 IC connector via the decade counter driver during the boards construction).
- The pulse generator switch of the clock input was pushed, and the states of the indicator LED and 7 segment displays were recorded. This step was repeated eight times.
- The experiment was done with both the 7447 and 74LS decoder drives, with the different supply voltages.

Result: The result obtained for the experiment is shown in the table below.

Table 4.9 4518 decade counter test result

Clock input state	Enable input state	Reset input state	Indicator LED states				7 segment display state
			Q_A	Q_B	Q_C	Q_D	
-	ON	ON	OFF	OFF	OFF	OFF	0
First push	ON	OFF	ON	OFF	OFF	OFF	1
2nd push	ON	OFF	OFF	ON	OFF	OFF	2
3rd push	ON	OFF	ON	ON	OFF	OFF	3
4th push	ON	OFF	OFF	OFF	ON	OFF	4
5th push	ON	OFF	ON	OFF	ON	OFF	5
6th push	ON	OFF	OFF	ON	ON	OFF	6
7th push	ON	OFF	OF	ON	ON	OFF	7
8th push	ON	OFF	OF	OFF	OFF	ON	8
9th push	ON	OFF	OF	OFF	OFF	ON	9

Discussion: The result obtained from the experiment satisfies the truth-table of the decade counter in table 3.8. The 7447 decade counters driver only worked with +5v supply. This shows that the CMOS logic can operate over a wider range of voltage supply than TTL. The experiment demonstrates the operation of the 4518 decade counter.

Chapter Five

Conclusions and Recommendation

5.1 Conclusion

The project work undertaken was the design and construction of a CMOS laboratory kit. The work took a period of about three months to finish as a whole. It begins with the research of the topic and gathering of literary materials needed to do the job. This was done in order to obtain a complete understanding of the topics.

The design of the work followed the research. The design was in two separate sections. This include the design of the power supply and the design of the laboratory kit board. The power supply involves the supply of power that would be compatible with the CMOS IC's on the laboratory kit board. The laboratory kit board, on the other hand, involves the circuits of the CMOS IC's that are to be tested and how it can be achieved.

The construction work then followed the design. The construction could be said to be the main project work (though it couldn't be achieved without the previous works). The construction involves the realization of the designs earlier outlined. Firstly, electric components were obtained before the actual construction took place. Some problems were encountered during the construction but were taken care off.

When the construction was finally completed, procedures were taken to test the work. This involves the investigation of the behaviour of the CMOS IC's on the laboratory kit. The results of the tests were quite satisfactory and aggress with what is expected. The procedures and result of the tests were properly documented.

Finally, it should be mentioned that the aims and objectives of the project were achieved.

5.2 Problems Encountered

As was mentioned above, some problems were encountered while constructing the project. These problems include the following:

i. Defective components:- Some components obtained for the construction were found to be defective in the course of the work and had to be replaced with good ones.

ii. Incorrect circuit connections:- Mainly due to human error and lack of much experience, some incorrect circuit connections were made during construction. At times it led to the damage of components and they are has to be replaced.

iii. Irregularity of power:- It is well known fact that supply of power in this country is irregular. This inevitably affected the construction and resulted in much unwanted delay.

5.3 Recommendation

i. Due to the inadequacy of laboratory equipments as well as the potentials of the CMOS laboratory kit, it is recommended that the department should have it. It will assist very much in the understanding of course like digital electronics and advanced circuit theory.

ii. It is also recommended that a battery power supply should be provided for use with the CMOS laboratory kit in order to counter the irregular supply of power.

iii. Lastly, it is highly recommended that the system of laboratory practical in the department should be definitely improved. The situation as it is now is not encouraging and leads to students' lack of sufficient experience during projects. And it is believed that better laboratory practical will definitely result in better student projects than there are now.

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