Automated Multiple Water Tanks Control System Using ATMEGA and FPGA Technology

Lukman Adewale Ajao, Blessing Olatunde Abisoye, James Agajo
Department of Computer Engineering
Federal University of Technology
Minna, Nigeria
ajao.wale@futminna.edu.ng,
b.abisoye@futminna..edu.ng,
james.agajo@futminna.edu.ng

Abdulzeez Olorundare Ajao
Department of Computer Engineering
Federal Polytechnic
Offa, Nigeria
ajaodoc@yahoo.com ng

Muhammed Bashir Mua'zu
Department of Computer Engineering
Ahamadu Bello University
Zaria, Nigeria
mbmuazu@abu.edu.ng

Abdulazeez Femi Salami
Department of Computer Engineering
University of Ilorin
Ilorin, Nigeria
salami.af@unilorin.edu.ng

***Abstract*— The automated multiple water tanks control system is designed and implemented for the usefulness of household, industries and manufacturing processes. Also, for the control and monitoring of water overflow or chemicals in the overhead tanks, as result of common wastage of water run-off from the overhead tanks. The system failure rate, and some relevant constraints are the challenges. It includes memory capacity, power consumption, wireless facilities and many others. The experimental design of this system was realized and demonstrated in the laboratory using ATmega microcontroller chip and FPGA technology. The proposed system experimentation was carried out to show the comparative performance of Field programmable gate array (FPGA) to its counterpart intelligent microchip (ATmega) application for industrial system manufacturing. In this research, an automated multiple water tanks control system was practically demonstrated in the laboratory to control the overflow and monitor the water level of the overhead tanks using ATmega 328 microchip, actuator (stepper motor), buzzer and others. The Xilinx 14.1 ISE was used for FPGA design, simulation and implementation on Spartan 6 FPGA development board. The experimental results from ModelSim simulator shows the system stability and efficiency which utilize total processing time of 4.99s, delay time of 6.557ns and total memory usage of 303192 kilobytes.**

Keywords—Actuator, Automated system, Intelligent microchip, Spartan-6 board, Water overflow

I. INTRODUCTION

The so-called overhead tank installation is mounted in the household for human's life sustenance and domestic activities, as well as farmland for irrigation and in the refineries for oil and gas processes [1, 2, 3]. The automated control and monitoring (ACM) of water lever in the overhead tanks require implementation of an Intelligent Pump Controller Circuit (IPCC) with integration of embedded sensors and wireless technology devices [4, 5]. This ACM component includes ultrasonic sensor and other related distance measurement or detection devices. The wireless communication devices are Bluetooth (BLE), ZigBee, WiFi, GSM etc, while actuator devices like water pump, stepper, servo or DC motor are involved. The programmable intelligent microchips (PIC) that control and coordinate all the activities of ACM system can utilized ATmega controllers (AVR), PIC series, 8051 family, PID controllers, Single-on-Chip (SoC), programmable logic device (PLD) and FPGA [1, 6].

This device (sensor and level indicator controller) is used for adequate monitoring of both liquid and gas volume in the reservoir. Some of the liquid level sensor are made with a metal plate which mounted on the overhead water tank to indicate top and lower level detection for the accuracy, efficient monitoring and to prevent overfilling [7, 8]. Level Indicator Controllers (LIC) is a device design with a long electrode strip to sense overhead liquid tank levels in the factories water tanks, housing, industries and manufacturing process [9].

An intelligent microchip or microcontroller is known as a small computer fabricated on a Single Integrated-Circuit (SIC), or it can be described as a Compact Integrated Chip (CIC) designed to control and coordinate an embedded system functions or operation. This CIC consists of numerous facilities that render some functions for the efficient system performance which includes microprocessor, memory (RAM and ROM), interrupt controller, analog-digital converter (ADC), timers, and input/output (I/O) peripherals on a single chip [10, 11].

Field programmable gate array (FPGA) are electrical interconnections of two-dimensional logic blocks array with switches and logic flip-flops. This FPGA device logic blocks implemented with multiple level of low fan-in gates to offer a compact design with two-level logic AND-OR gate [12]. FPGA is efficient to integrate thousands of logic gate in a single integrated circuit (IC), and widely applicable in industrial system control and manufacturing of embedded systems for high speed performance, memory constraint improvement and real time operations [13]. This monitoring and control system applications are important in the following areas; military, residential, industrial automation, industrial chemical process, transportation, network operation centers, power plants, agricultural areas, medical applications, and others.

The traditional way of measuring and monitoring liquid level or overflow in a tank (reservoir) is achieved using a long pipe or stick through the upper part of tank. Such that if the tank is filled up, the water overflow through the pipe hole will be indicated. But with recent development and approach of using artificial intelligence (AI) and embedded intelligent chip or single-on-chip (SoC) technology has made it possible for all these processes to be automated and monitor every activity remotely in a real-time [14, 15].

II. Related Works

There are many proposed methods for the liquid level monitoring and control system in literature with the use of microelectronics, digital electronics, and wireless communications technologies [16]. However, the utilization of non-automated system for ON and OFF of a pumping machine sometimes causes water overflows or wasteful electrical power consumption [17].

In [8], researchers describe the water level tank control in the thermal plants for resources management and domestic consumption. An FPGA approach is proposed for water level monitoring and control of the powered pump (ON) when the water in overhead tank is lower than the specified and turn (OFF) when it filled up to the upper level of water tank. In [18], authors developed a system that monitors the liquid level of industrial tanks using an ultrasonic sensor. At each segment or water tank level, the sensor senses and take precaution by sounding alarm and control the system when it reached the specified levels. The use of economical water tank control system using Arduino UNO microcontroller was explained in [19], and ultrasonic sensor for liquid levels detection which is interfaced with LabView software. The front panel of LabView display the liquid level of the tank and the powered-motor status (ON or OFF).

The importance of water to the human race as well as other living creatures, and the need to optimize its usage to avoid wastage is discussed in [20]. This system was implemented using an automatic water level indicator with a microcontroller to monitor the water conductivity because of the presence of minerals within it. As the water level rises or falls, the controller sends out different signals as indicator. These signals are used to control switching ON and OFF of the motor integrated to water pump as specified in the coding. This system is controlled in auto mode to turn ON when water level rise to 20% and OFF when water level rises to 100% as demonstrated in [21, 24].

A contactless non-intrusive ultrasonic based liquid level monitoring and control system was proposed in the research of [22]. The system operations were based on the reflective property of ultrasonic wave principle. The liquid surfaced is measured while the sensor intercepts with the reflected wave, and compute the distance of the liquid level from the sensor. A programmed microcontroller uses the data acquired from the sensor to concurrently monitor the water level of both an overhead tank and underground reservoir tanks [25]. From the results obtained shows the optimal performance, efficiency and correlation between the simulated result and the implemented system prototype.

One of the most recent implementation technologies for overhead water tank remote control, monitoring and surveillance is implemented in [26, 27]. The application of this recent discovery; Artificial Intelligence (AI) and Computational Intelligence (CI) such as Fuzzy logic, artificial neural network, genetic algorithm, particle swamp optimization and many others are proposed in [28, 29, 30] for the optimization and efficient performance of the overhead water tank control and monitoring.

The author contributions in this research focus on hands-on laboratory implementation for automated multiple water tanks control and volume monitoring using ATmega intelligent microchip as discussed in section III. Also, Section IV described an efficient method of implementing automated multiple water tanks control and volume monitoring for the large-scale industries production and manufacturing processes using FPGA technology. This technology (FPGA) proves efficient for industrial applications with the following advantages, metrics and features includes Non-Recurring Cost (NRE), processor speeds memory in giga-hertz (GHz), relative low power consumption, multiple wireless facilities support (BLE, WiFi, Ethernet etc), high clock speed in Mega-Hertz (MHz), large programmable block and IO block and support of reprogrammed and many others. The comparative performance of FPGA technology to conventional microcontroller like AVR microchip architecture are highlighted in section V.

III. Automated System Design and Implementation

A. Laboratory Implementation of Automated Multiple Water Tanks Control using Atmega328

In this paper, Arduino Uno microcontroller (Atmega328) and ultrasonic sensor (HC-SR04) are used basically for the laboratory experimental prototype to detect and monitor the liquid level of overhead water tanks. Stepper motor was used for control of the water tank system (ON/OFF). Such that if two or more tanks are filled up with liquid the buzzer sound alarm and activate yellow light indicator. Therefore, for the comparative performance of this automated system implementation in the manufacturing process or an embedded system industry, FPGA technology is proposed to take advantage of microcontroller placement in the system circuit. This is due to its capacity, efficient performances, memory capacity, wireless facilities, CPU utilization, system response time (speed), and power consumption in the process of control and monitoring activity. This system is experimented and implemented in the laboratory as illustrated in “Fig. 1”.

Some of the components employed in the system are Arduino Uno board integrated with ATmega328 MCU, relay, buzzer, ultrasonic sensor (HC-SR04), and multiple tanks with actuator. The liquid level in the tanks are detected as (HIGH or LOW) with an indication light display. The green light indicates the beginning of liquid level in the first two tanks, which induce the voltage level of the system to HIGH causing actuator to maintain power ON in the pumping system. The yellow light indicate that two or more reservoir liquid level is filled up and the red-light glow when the liquid level of the last reservoir is reached the peak level causing the voltage level of the system to change state to LOW by activate the buzzer and turn OFF the actuator pumping system. The embedded system circuit diagram for multiple water tank control is programmed and simulated in the Proteus Virtual Simulation Model (PVSM) using Atmega328 microchip as demonstrated in "Fig. 2", and system operation flowchart is given in "Fig. 3".

Figure 1: Automated multiple water tanks control and implementation

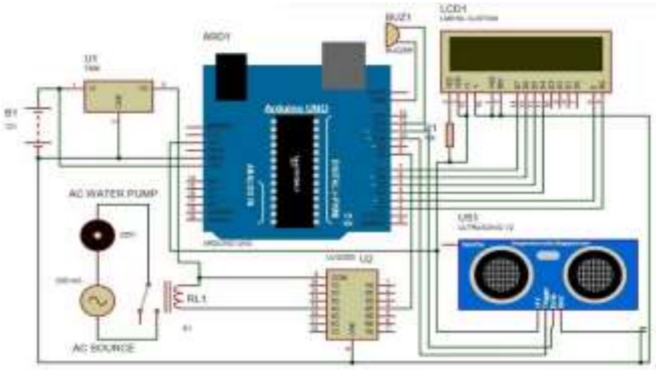

Figure 2: Automated system circuit integration in PVSM

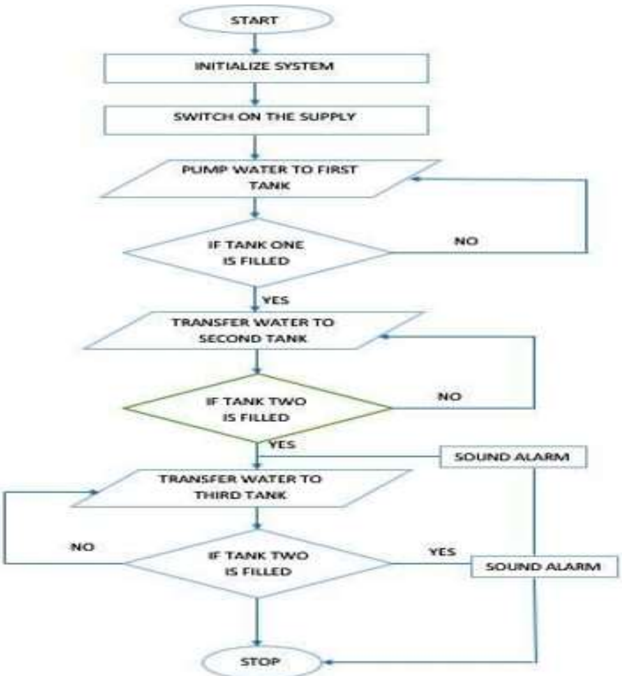

Figure 3: Automated system operation flowchart

B. *Automated Multiple Water Tanks Control System with HC-SR04 Ultrasonic Sensor*

The Three relative ultrasonic sensors were used to sense the water level of the different tank and buzzer was connected in the circuit to generate the alarm sound for signaling of two or more tanks filled up. When the system is powered ON, water is pumped and flow through tank1 until it reaches the height stage. The system recorded as tank1 filled up but does not activate alarm. At this point, the water flow from tank1 through tank2 until the water level reaches the peak of tank2, then the system registers increment means both tank1 and tank2 are filled up which trigger an alarm to indicate that two or more tanks are filled up. This process continues until tank3 filled up is detected by the LIC and sensor, which trigger the circuit and water supply is cutoff to end the processes.

The HC-SR04 ultrasonic sensor is designed with 4-pins which are Ground (GND), Power (VCC), Triger (Trig) and Echo which is used to determine the distance of liquid level in the tanks. The GND and VCC pins are connected to the Ground and to the 5volts pins of the Arduino Board respectively, while the trig and echo pins are connected to digital I/O pin of the Arduino board.

The distance of the liquid level can be determined and computed by measuring the total time travel between the sensor and liquid level, not by the intensity of the sound. Where dx and dt are denote certain distance between the sensor and the travel time of incident and reflected wave in the tank respectively as illustrated in "Fig. 4". The HC-SR04 ultrasonic sensor uses the distance between the sensor and the product surface to calculate the liquid level in a tank as expressed in "(1)".

$$Distance\ (d) = \frac{Speed\ of\ sound\ (u) * time\ delay\ (t)}{2} \qquad (1)$$

C. *Automated Multiple Water Tanks Control System with HC—SR04 Ultrasonic Sensor*

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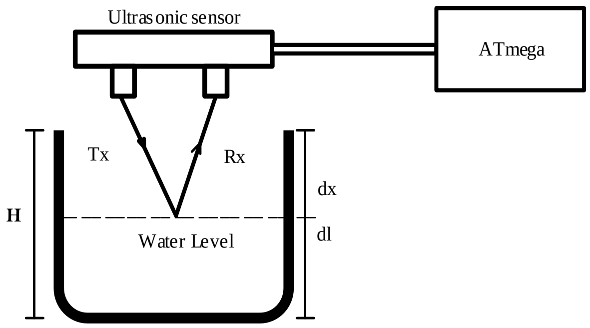

Figure 4: Ultrasonic sensor implementation in a reservoir.

The summation time of flight of the sensor between levels of the liquid to the receiver is computed as 2dx. Therefore, the speed (ü) of wave is expressed as in "(2)", where changes in distance (dx) of liquid level is expressed as in "(3)" and "(4)".

$$\ddot{u} = \frac{2dx}{dt} \quad (2)$$

$$dx = \frac{\ddot{u}dt}{2} \quad (3)$$

$$\int dx = \frac{\ddot{u}}{2} \int dt \quad (4)$$

The given speed of sound in air is approximately to 340m/s, the instantaneous distance between the liquid level and sensor with respect to time of flight t is calculated as in "(5)".

$$x = \frac{340 m s^{-1} \times dt}{2} = 170 m/s \quad (5)$$

Also, H is the maximum height of tank and υ is the volume of the liquid in the tank, then it is expressed as in "(6)" and "(7)", where k is constant of proportionality.

$$dl = h - dx \quad (6)$$

$$\upsilon = kdl \quad (7)$$

IV. FPGA—BASED AUTOMATED MULTIPLE WATER TANK CONTROL SYSTEM: DESIGN AND IMPLEMENTATION

A. Digital Logic Design for Multiple Water Tanks Control

The FPGA configuration is generally specified using hardware descriptive language (HDL), similar to the application-specific integrated circuit (ASIC). It is a two-dimensional arrays of logic blocks and flip-flops with an electrically programmable interconnection between logic blocks routing channels. The industrial multiple reservoir control and monitoring system is proposed and implemented as illustrated in "Fig. 5", using field programmable gate array (FPGA) for the efficient performance, low power consumption and memory utilization.

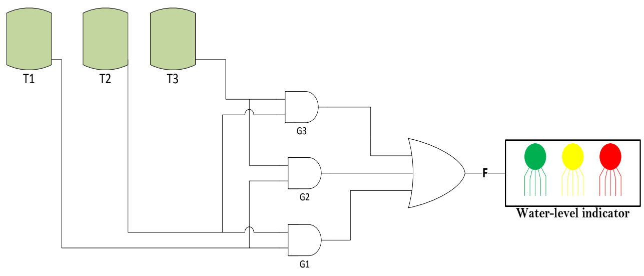

Figure 5. FPGA-based multiple reservoirs logic circuit

The Boolean logic expression of the system behaviors is computed in the expression given of "(8)" and "(9)", and the system logic behavior algorithm described as follows.

$$F_o = T_1T_2 + T_1T_3 + T_2T_3 \quad (8)$$

$$F_o = T_1(T_2 + T_3) + T_2T_3 \quad (9)$$

System Logic Algorithm

1. *Initialize the system*
2. *Power ON the system*
3. *Control the water tap (Open)*
4. *Pump water to the tank 1*
5. *IF (Q SET is active)*
6. *THEN make Q state to be HIGH--- Green Light ON*
7. *If two or more water tank is filled*
8. *ELSE the Q state REMAIN--- Yellow Light (ON)*
9. *IF the last tank is filled*
10. *ELSE IF (Q RESET is active)*
11. *Control the water tank (Closed tap)*
12. *THEN make Q state to be LOW--- Red Light ON and Alarm*
13. *ELSE the Q state remain constant*
14. *Continue alarm sound*
15. *End **if***
16. *End*

B. VHDL Coding for Multiple Tanks Control

This system was also developed with Very High-Speed Integrated Circuit Hardware Descriptive Language (VHSIC-HDL), which comprises of library, entity and architecture declarations. In the process of hardware descriptive language synthesis consists of coding in VHDL module and testbench which they are Netlisted to generate waveform result in the modelsim environment.

VHDL Module for Multiple Tanks Implementation

1. *Library IEEE;*
2. *Use IEEE.STD_LOGIC_1164.ALL*

```

Entity FiveTanksAlarmHDL is
Port(
tank1, tank2, tank3, tank4, tank5 : in STD_LOGIC;
OUTPUT : out STD_LOGIC);
End FiveTanksAlarmHDL;

Architecture Behavioral of FiveTanksAlarmHDL is
begin
OUTPUT <=(NOT ((((NOT tank1) AND (NOT
tank2) AND (NOT tank3))AND(tank4 XOR tank5))
OR (((NOT tank3) AND (NOT tank4) AND (NOT
tank5)) AND (tank1 XOR tank2)) OR ((NOT tank1)
AND (NOT tank2) AND (NOT tank4) AND (NOT
tank5))));
End Behavioural;
```

C. FPGA Architecture and Implementation

The FPGA implementation for industrial chemical or water tanks control and monitoring is proposed and simulated using Xilinx 14.1 ISE field programmable gate array and implemented on Spartan-6 development board using (XC6LX16-CS324). The simulated waveform result is achieved through the Xilinx modelsim, due to low static power consumption during operations with 16MB of parallel PCM, cellular RAM and x4 SPI PCM features. This help to achieve inputs slices of LUT-4 (Look-Up-Table-4) technology for industrial chemical tanks implementation, and core logical function of the system. Which can be described as 2- XOR input logic with integration of others input Chi logic. This chi logic includes XOR, AND, OR, and NOT Boolean logical operation. All of these input logics are contained and stored in a single LUT-4 primitive which used as a signal control selection between the identified chi logics and 2-input XOR logic gate. The FPGA Spartan-6 architecture board also consists of some features like USB port for user data configuration, 8-bit VGA, USB-UART connection port, USB human interface device (HID), 10-100GB Ethernet connection, basic input and output and high-speed expansion port as illustrated in "Fig. 6", and details of its efficient performance is discussed in [31].

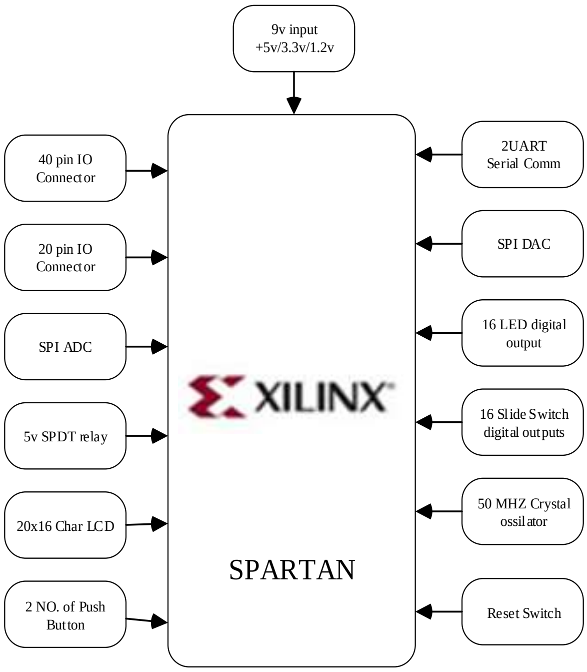

Figure 6. FPGA spartan-6 block diagram features.

V. FPGA TECHNOLOGY SIMULATION RESULTS

A. Register Transfer Logic Implementation and Simulation

The FPGA based multiple water tanks control was designed and implemented in Xilinx ISE 14.0, and the waveform result was achieved through ModelSim. The register transfer logic (RTL) schematic is shown in "Fig. 7", and wave form result after simulation in Modelsim are illustrated in "Fig. 8". The multiple overhead water tanks are presented as input, while the output shows the situation of water level in the multiple tanks which connected together with buzzer for alarm. From the result obtained shows that, the output voltage goes high whenever two or more tanks goes HIGH and change the state to LOW when two or more tanks fall below specified level.

Table 1 illustrate the data sheet report of gate delay that existing between the source pad and destination pad during simulation. Table 2 shows the design summary and analysis of memory utilization, CPU time and path delay during logic synthesis. "Fig. 9" illustrate its graphical representation.

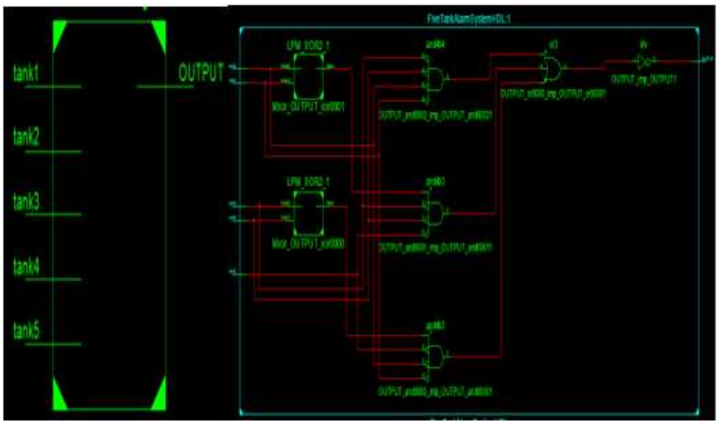

Figure 7. RTL internal and external architecture of the system

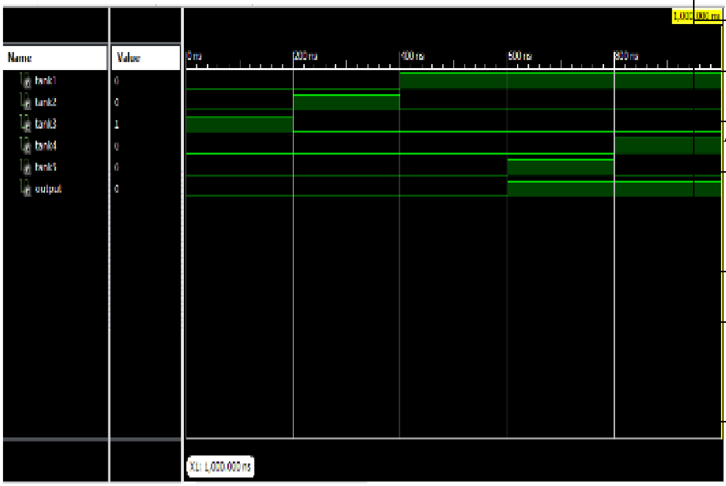

Figure. 8. Waveform result for multiple tanks monitoring

TABLE I. DATA SHEET REPORTS FOR MULTIPLE TANKS SIMULATIONS

Source pad	Destination pad	Delays (ns)
Tank 1	Output	7.638
Tank 2	Output	6.799
Tank 3	Output	6.891
Tank 4	Output	6.847
Tank 5	Output	6.805

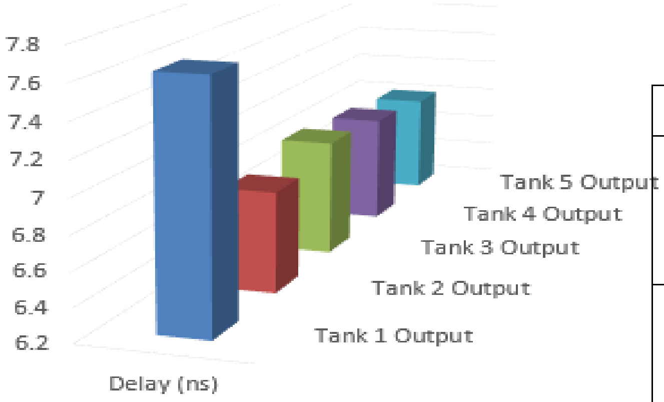

Figure 9: Logic gate delay (ns) against simulation output tank response

TABLE II. DATA SHEET REPORTS FOR MULTIPLE TANKS SIMULATIONS

Logic utilization and distribution	0	Delay (ns)
Number of 4 input LUTs	2 of 9,312	1%
Number of occupied slices	1 of 4656	1%
Number of slices containing for related logic	1 of 1	100%
Number of slices containing for unrelated logic	2 of 9312 (4-LUTs)	1%
Number of IOs	6	-
Number of IOBs bonded	6 of 232	2%
Average Fan-out of Non-clock	1.67	6.805
Maximum combination path delay	6.557ns	-
Peak memory usage	303192 KB	
Total CPU time to Xts completion	4.99 ecs	

B. *Comparison Performance Between FPGA and ATMEGA Microcontroller Chip Architecture*

The architecture of the Field Programmable Gate Array (FPGA) based on Spartan-6 board was studied and compared with this conventional intelligent AVR-ATMEGA microchip as analyzed in Table 3. These intelligent technologies application for embedded system purposes can be measured with the following metrics or tradeoff. It includes cost, performance and power-effective tradeoff between them. Of course, as a result of reprogram ability of FPGA technology to fit any logic design with the same number of gates reduce the cost of industrial products unlike conventional MCU that are used for specific application. It has better performance in terms of processor speed, large memories and relative low power utilizations.

TABLE III. FPGA VERSUS ATMEGA MICROCONTROLLER

FPGA technology	ATmega microcontroller
Faster-time-to-market: it does not require special layout or any manufacturing procedures in the design	Slower-time-to-market: it required specific design layout for device manufactured.
High clock speeds in hundreds of MHz: It operate at high speeds frequency of (50-600) MHz (Faster)	Low clock speeds: It operate at low frequency range from (8-16) MHz with voltage level of (3-5) V respectively (Slower).
It has large programmable block and IO block	No programmable blocks
It is Non-recurring expenses (NRE): a one-time cost to system design, test of a new product and product enhancement.	It is costly and expensive for the re-engineering product and product optimization or enhancement.
It supports large memories with	The memories capacity is low

maximum data rate of different speeds; 2667Mb/s, 2400Mb/s, 1866Mb/s, 8000Mb/s range for storage of industrial application and functions	are in kilobyte
It required simple design cycle: Since the routing, placement and timing is handle by the software.	The design cycle take time.
Field programmable: capable of reprogrammed to suit any logic design fitted to the number of gates possess.	Application-specific: programmed for some simple tasks of hardware.

VI. CONCLUSION

An industrial automated multiple water reservoirs control and volume monitoring system was developed and implemented in the laboratory using ATmega328 microchip. It was tested and proved to be efficient in the real time control and monitoring of overhead water tanks level. This approach actually manages the overhead water wastage in the household and other areas of application. But, this intelligent microcontroller (ATmega328) for industrial application has shortage lifetime, hazard rate function as a result of its flexibility, mean-time-to-failure, (MTTF), inherent weakness and other environmental conditions (includes heat, temperature and so on). The FPGA technology approach for automated multiple water tanks control and volume monitoring was implemented and simulated in the Xilinx ISE. This technology (FPGA) application is suitable for the industrial control system, since it exhibited many advantages over the microcontroller. It includes extremely low power consumption, efficient CPU utilization, memory capacity, extended system features for various applications and multiple wireless technology. It has high resistant of failure rate due to reliability predication, extended failure time distribution and gradual failure time characteristics. This was implemented and tested which proves to be efficient and quick responds. This research work can be extended and adopted in industries to monitor and control the volume level of liquids such as kerosene, diesel and other crude oil using FPGA or fuzzy controller for an improved performance.

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